

Storm 2
UMA Schematics Document

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Storm2

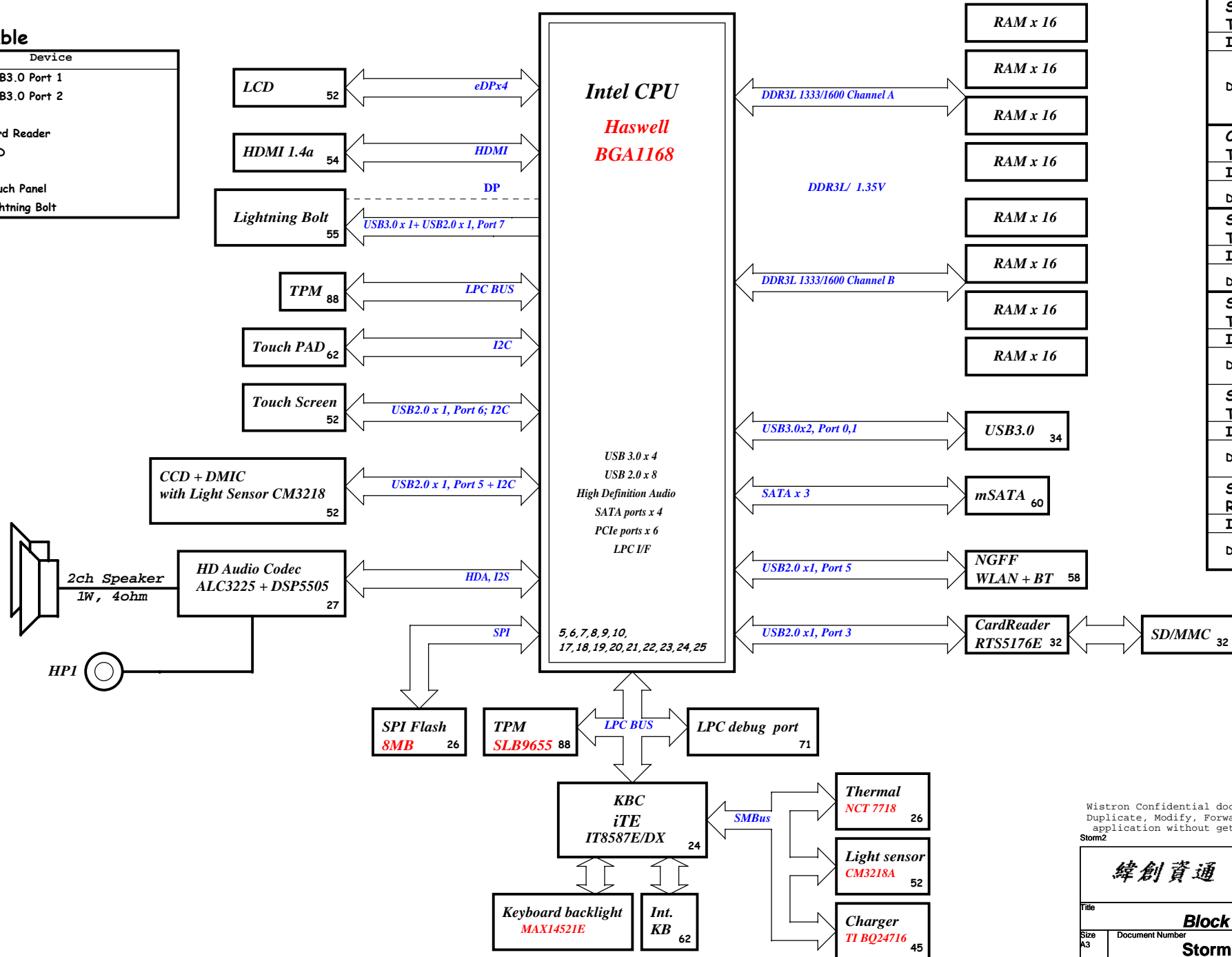
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Cover			
Size	Document Number		Rev
A4	Storm 2		-1
Date: Wednesday, March 13, 2013		Sheet 1 of	102

Project code : 91.4LZ01.001
PCB P/N :12302-1
Revision : 1

Storm 2 Block Diagram

USB Table

Pair	Device
0	USB3.0 Port 1
1	USB3.0 Port 2
2	NA
3	Card Reader
4	CCD
5	BT
6	Touch Panel
7	Lightning Bolt



CHARGER BQ24737 44	
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC TPS51285 45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_DSW 3D3V_WLAN_S0 MSATA_VDD MSATA_VDD 5V_DSW 5V_S5 USB30_VCC
CPU DC/DC TPS51622 46, 47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC TPS51367 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC TPS51367+TPS51206 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 VDDQ_VREF 0D675V_S0
SYSTEM DC/DC TLV62065 51	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0
SYSTEM DC/DC RT9013 58	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0

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Title Block Diagram	
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SSID = CPU

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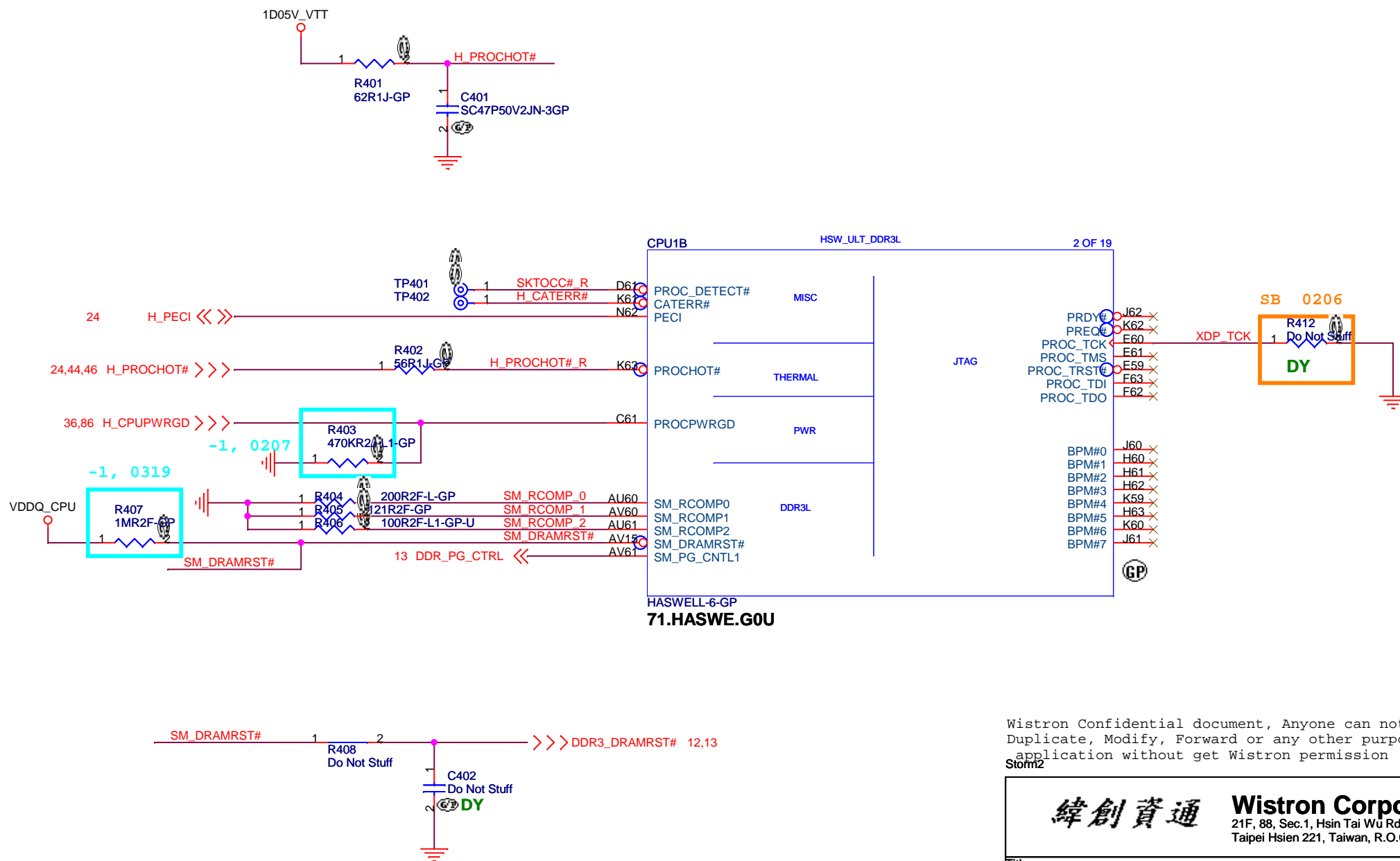
緯創資通

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Title
CPU (Reserved)

Size A4	Document Number Storm 2	Rev -1
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SSID = CPU



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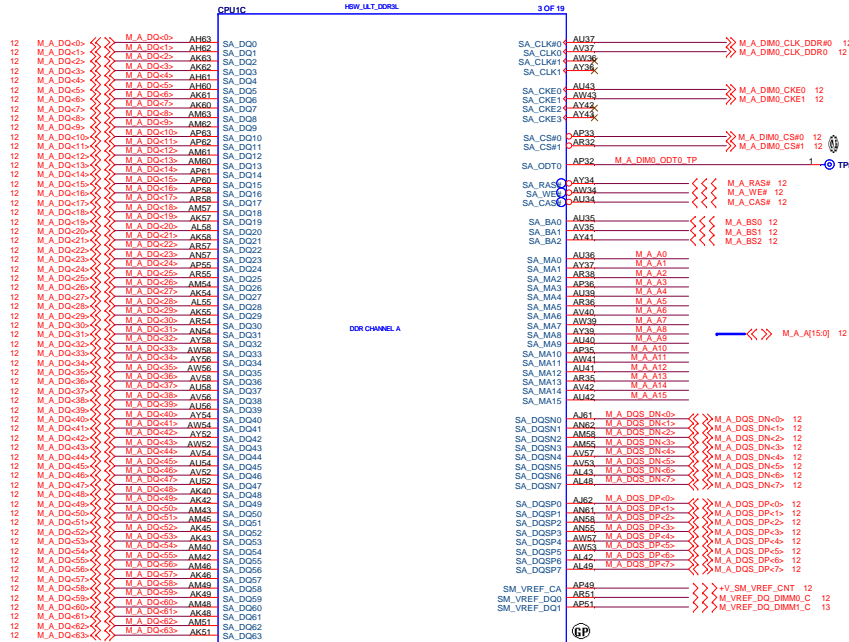
緯創資通 **Wistron Corporation**
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Title	CPU (THERMAL/CLOCK/PM)
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Size A4	Document Number Storm 2	Rev -1
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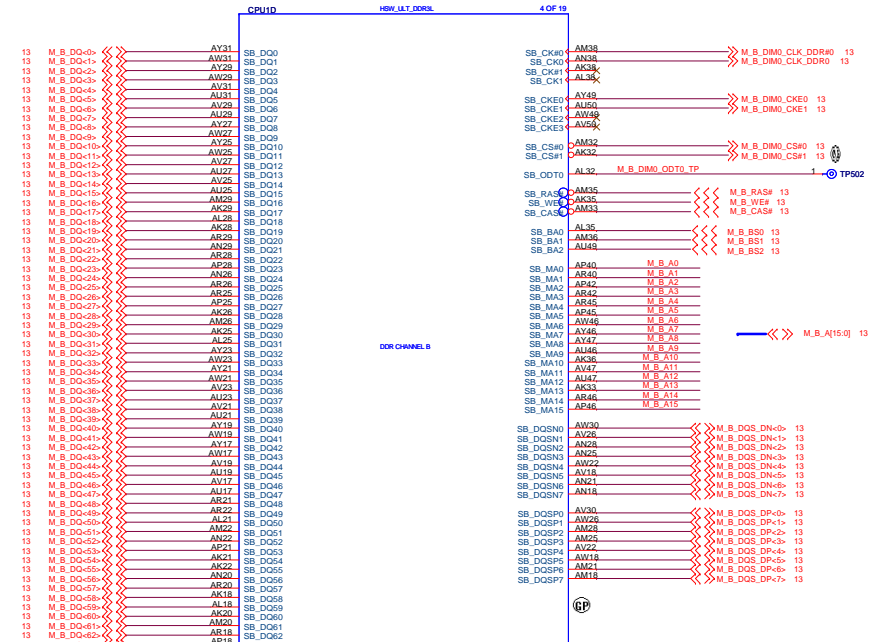
Date: Tuesday, April 02, 2013 Sheet 4 of 102

SSID = CPU



HASWELL-6-CP

71.HASWE.G0U

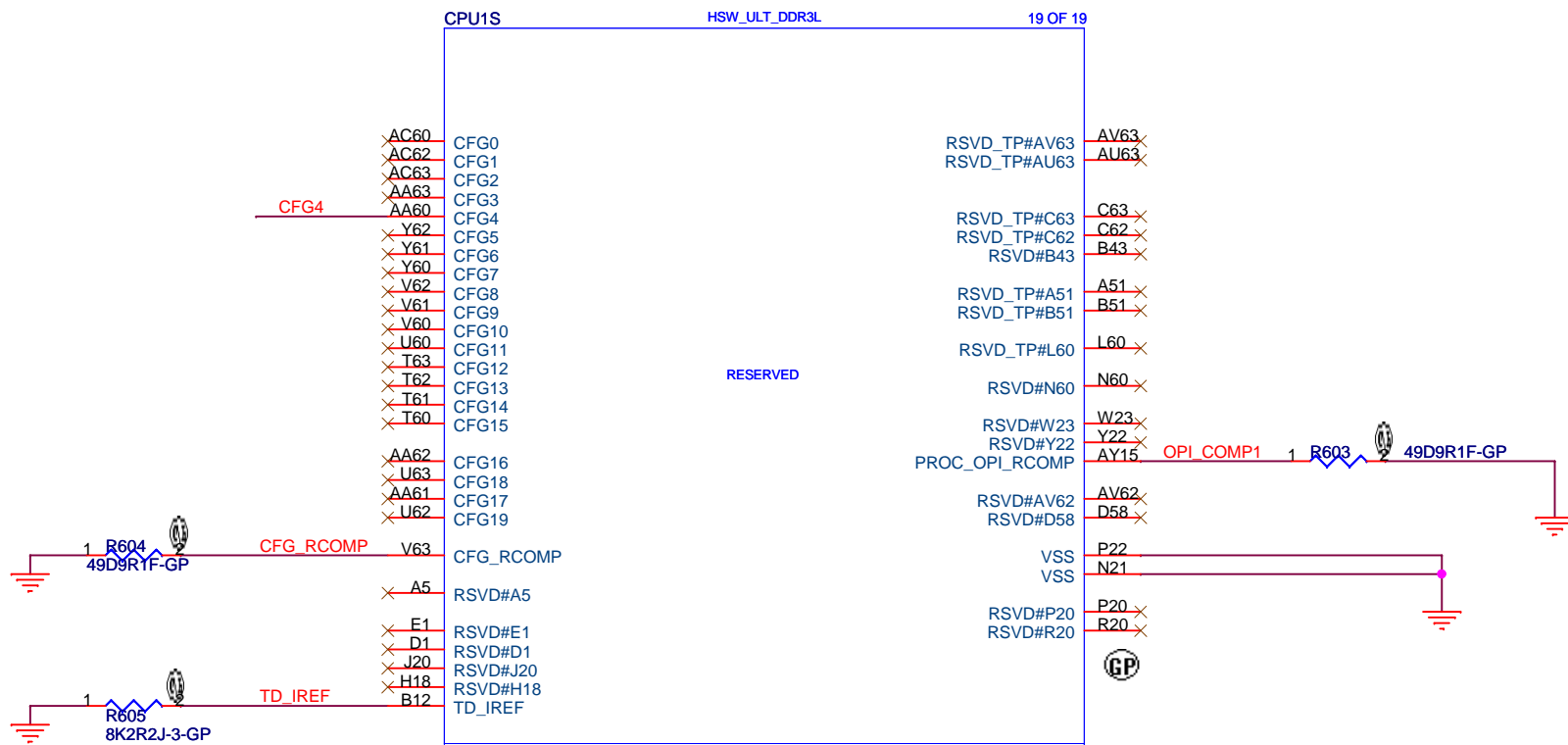


HASWELL-6-CP

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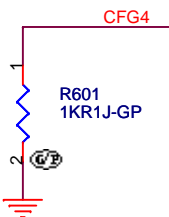
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Title CPU (DDR)	
Size A2	Document Number Storm 2
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SSID = CPU



71.HASWE.G0U

eDP Enable	
	1:Disable
CFG4	0:Enable



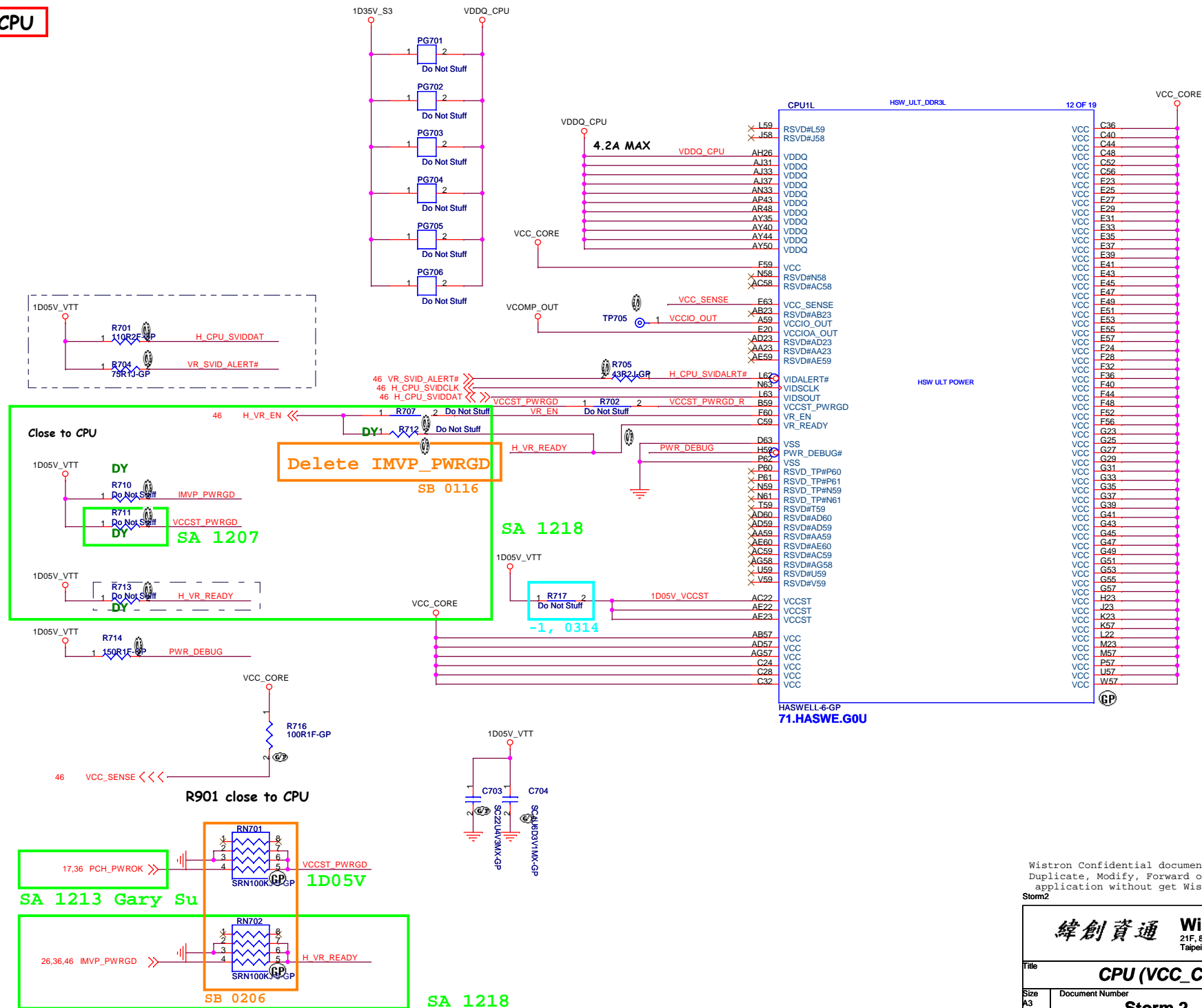
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Title CPU (CFG)		
Size A4	Document Number Storm 2	Rev -1
Date: Friday, December 28, 2012 Sheet 6 of 102		

SSID = CPU



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Title			
CPU (VCC_CORE)			
Size A3	Document Number		Rev
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SSID = CPU

HDMI

54 DDBP_DATA2#
54 DDBP_DATA2
54 DDBP_DATA1#
54 DDBP_DATA1
54 DDBP_DATA0#
54 DDBP_DATA0
54 DDBP_DATA3#
54 DDBP_DATA3

55 DP_DATA0#
55 DP_DATA0
55 DP_DATA1#
55 DP_DATA1
55 DP_DATA2#
55 DP_DATA2
55 DP_DATA3#
55 DP_DATA3

Lightning Bolt

CPU1A

HSW_ULT_DDR3L

1 OF 19

C54 DDI1_TXN0
C55 DDI1_TXP0
B58 DDI1_TXN1
C58 DDI1_TXP1
B55 DDI1_TXN2
A55 DDI1_TXP2
A57 DDI1_TXN3
B57 DDI1_TXP3

C51 DDI2_TXN0
C50 DDI2_TXP0
C53 DDI2_TXN1
B54 DDI2_TXP1
C49 DDI2_TXN2
B50 DDI2_TXP2
A53 DDI2_TXN3
B53 DDI2_TXP3

DDI

EDP

EDP_TXN0
EDP_TXP0
EDP_TXN1
EDP_TXP1

EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUXN
EDP_AUXP

EDP_RCOMP
EDP_DISP_UTIL

C45 CPU_EDP_DATA0# 52
B46 CPU_EDP_DATA0 52
A47 CPU_EDP_DATA1# 52
B47 CPU_EDP_DATA1 52

C47 CPU_EDP_DATA2# 52
C46 CPU_EDP_DATA2 52
A49 CPU_EDP_DATA3# 52
B49 CPU_EDP_DATA3 52

A45 CPU_EDP_AUX# 52
B45 CPU_EDP_AUX 52

D20 EDP_RCOMP
A43



VCOMP_OUT
R801
24D9R2F-L-GP

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Title

CPU (DDI/EDP)

Size
A4

Document Number

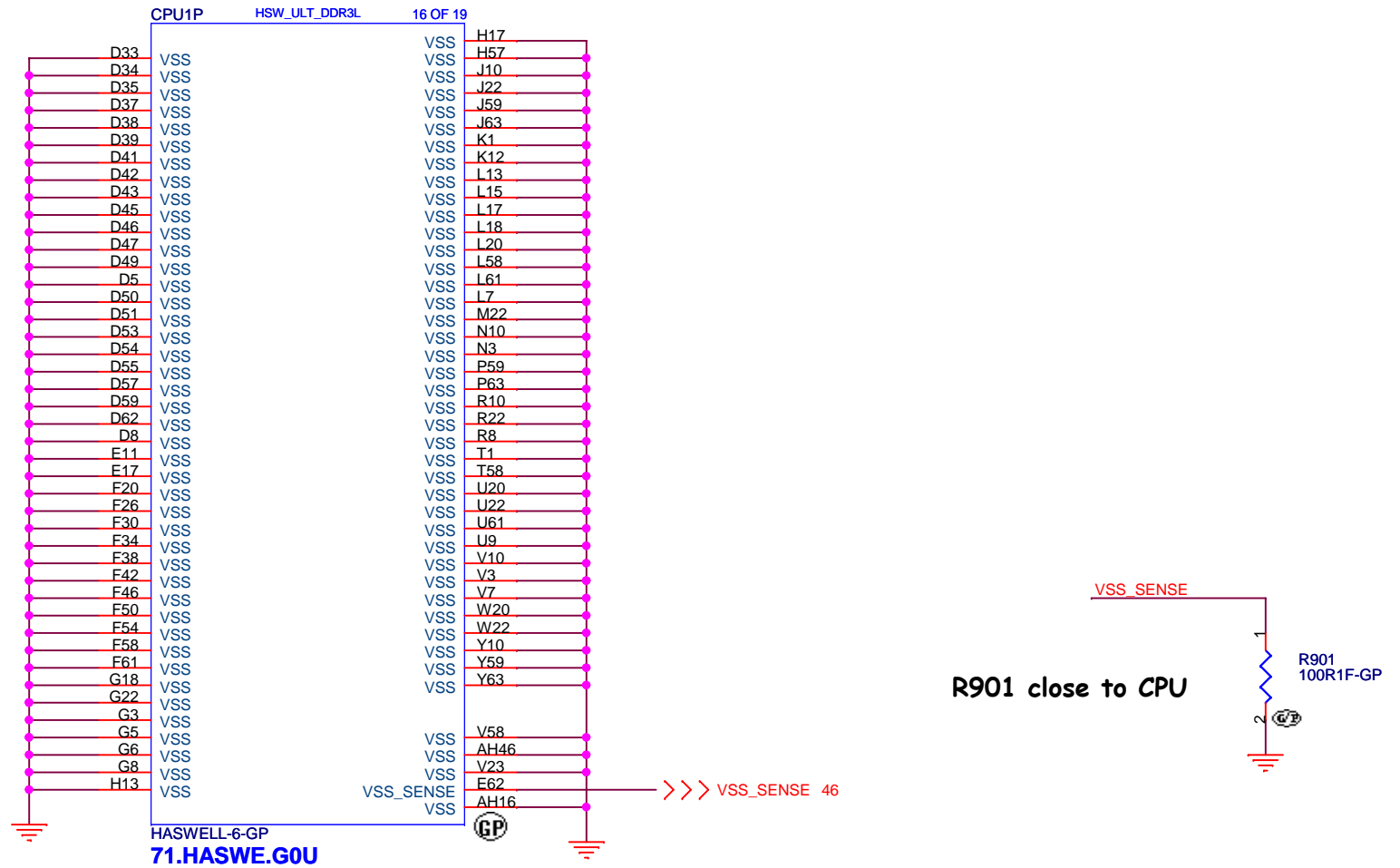
Storm 2

Rev
-1

Date: Tuesday, April 02, 2013

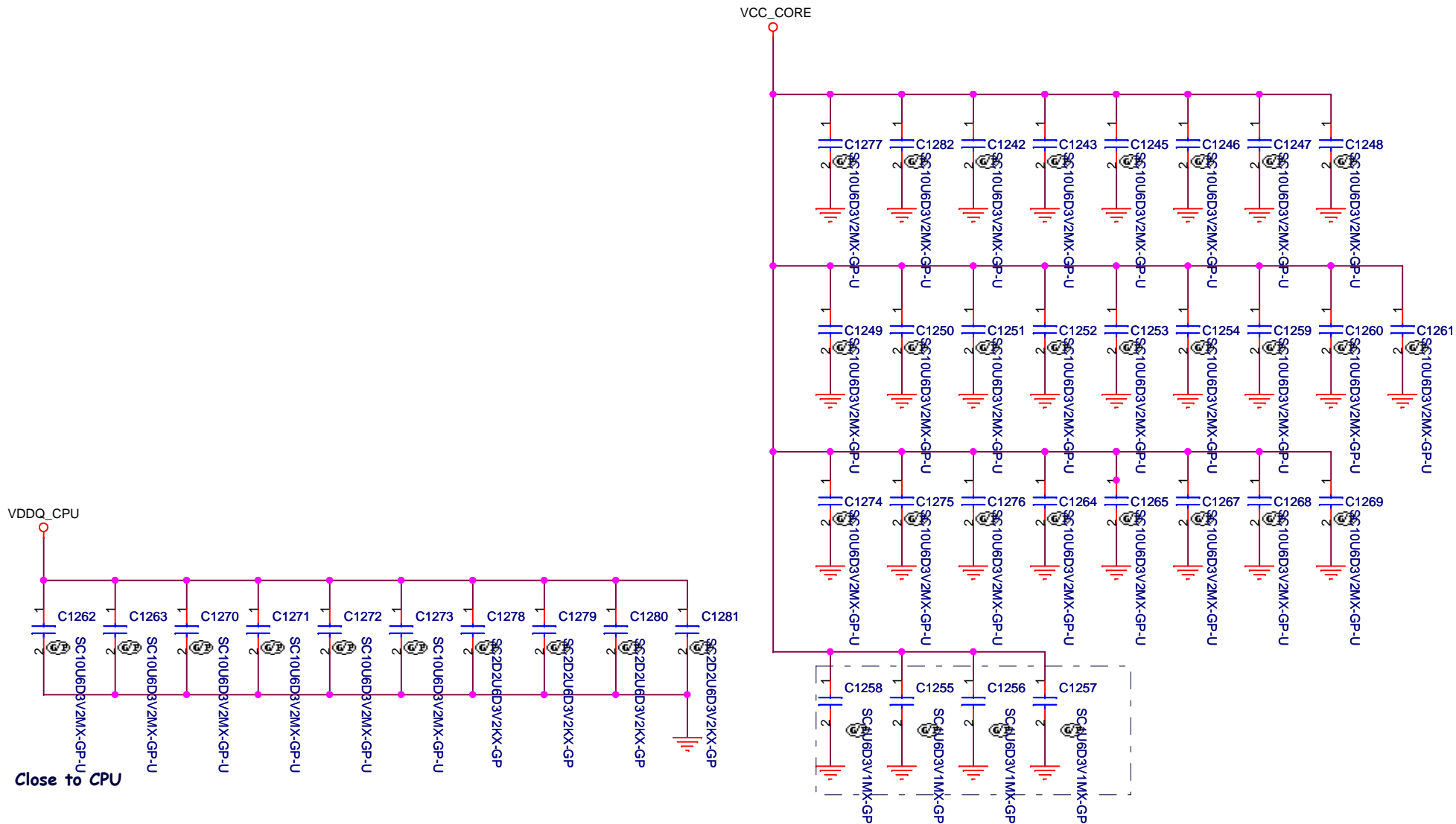
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SSID = CPU



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Title CPU (VSS)		
Size A4	Document Number Storm 2	Rev -1
Date: Tuesday, April 02, 2013	Sheet 9	of 102

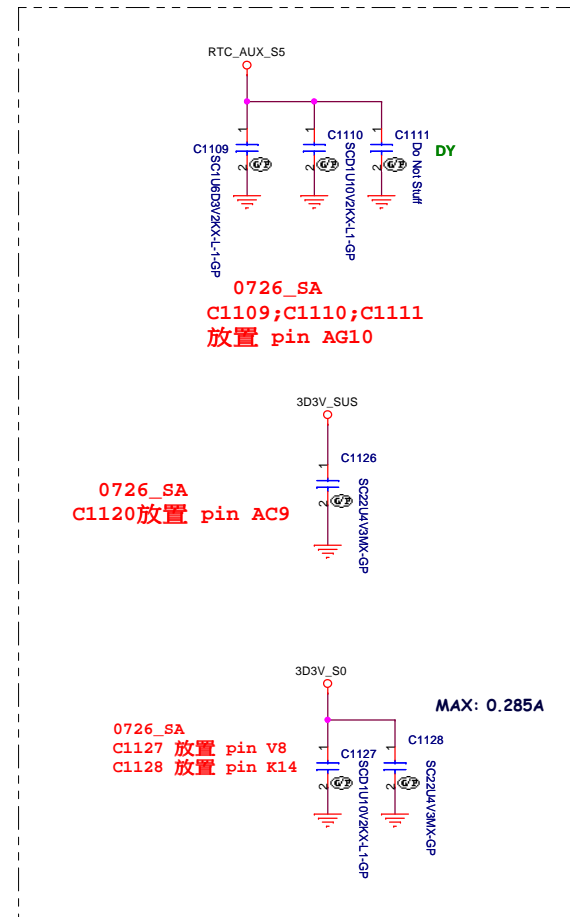
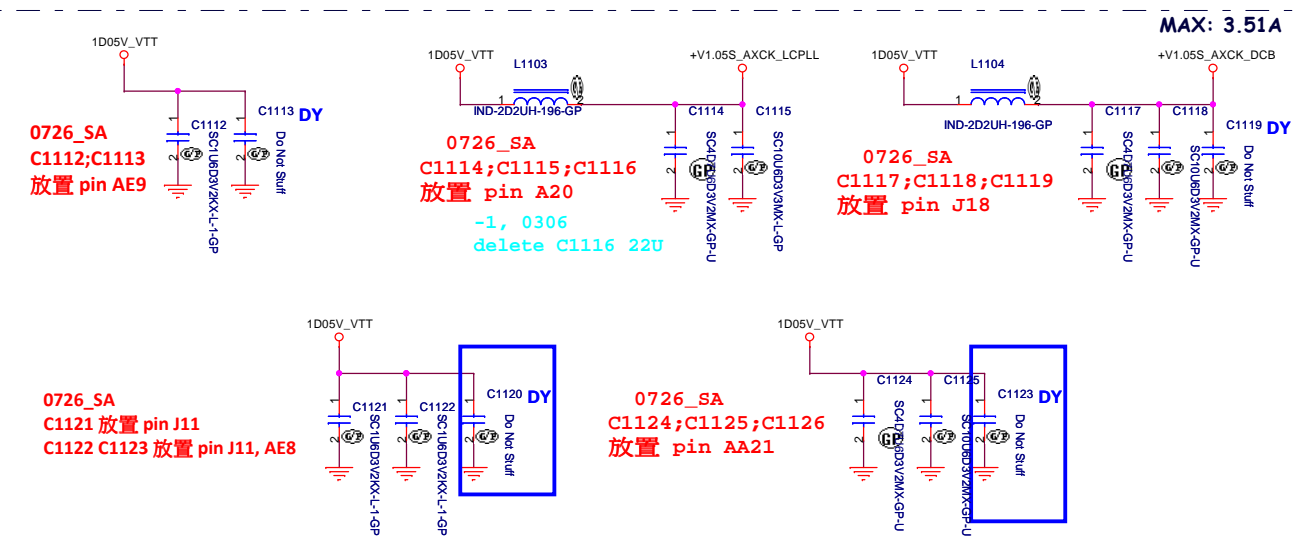
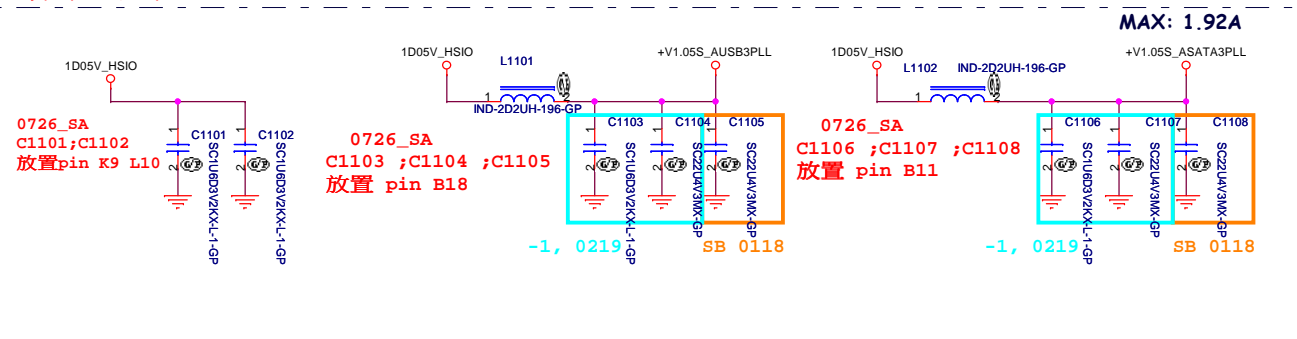


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TitleCPU (Power CAP1)		
SizeA4	Document NumberStorm 2	Rev-1
DateMonday, February 04, 2013	Sheet10	of102

0726_SA 擺放電容的位置請參考Page 21
每個位置如下

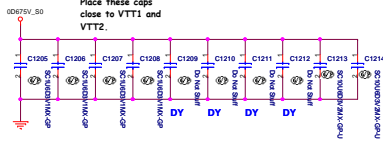
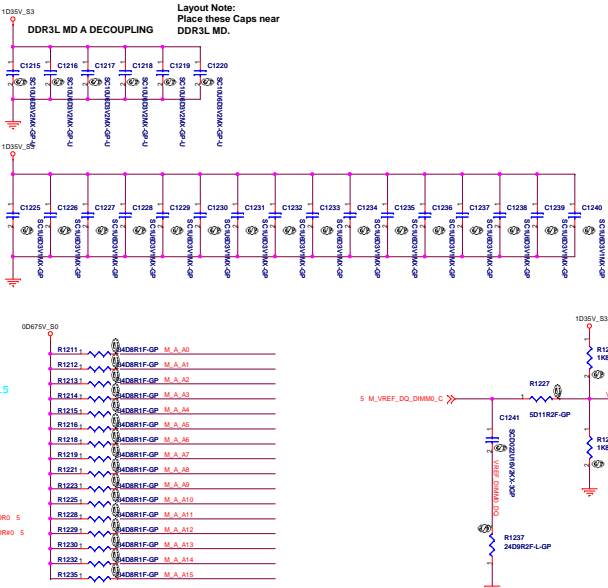
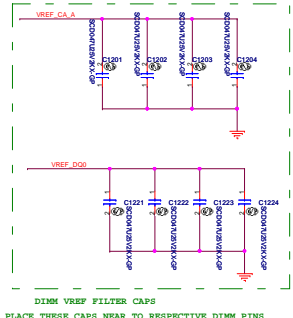
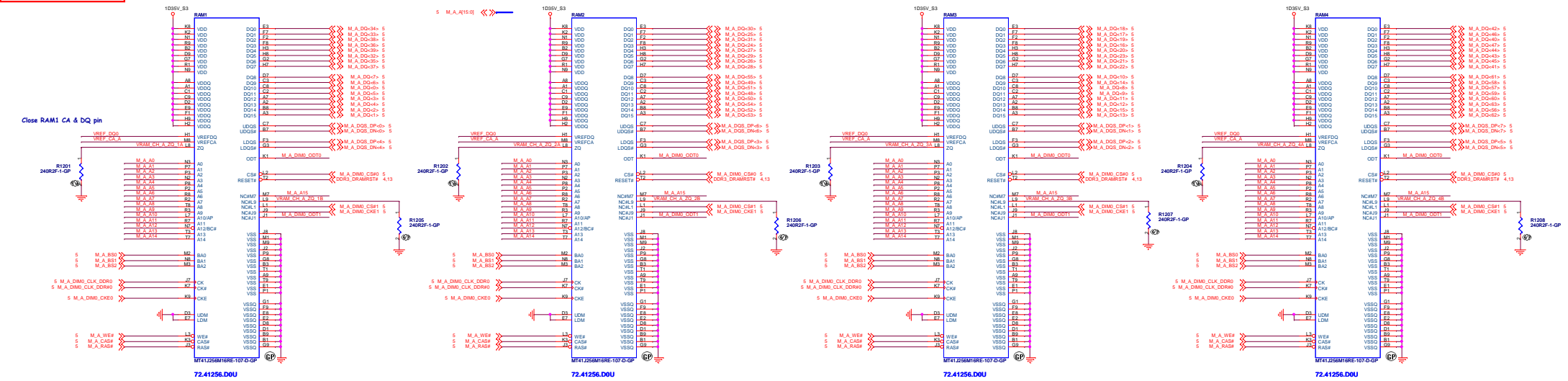


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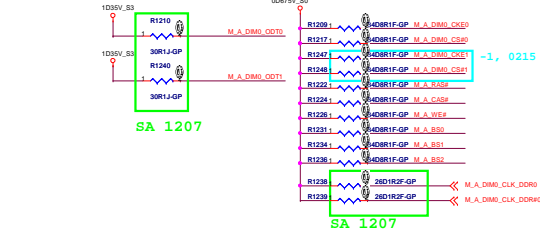
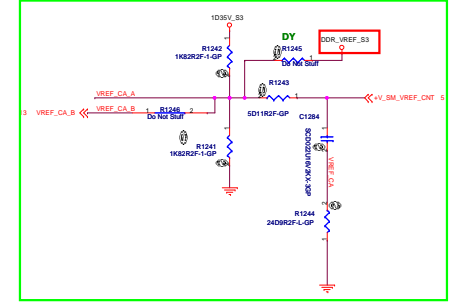
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Title	<i>PCH (Power CAP2)</i>
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SA 1207

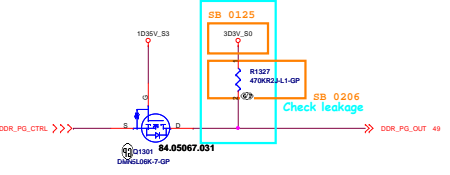
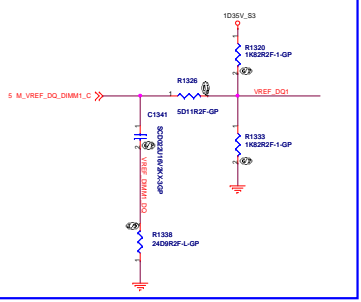
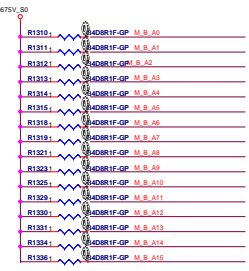
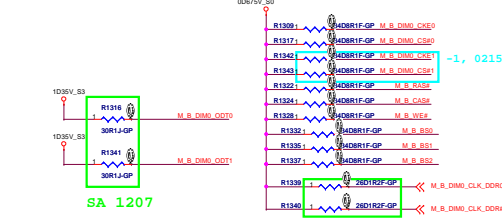
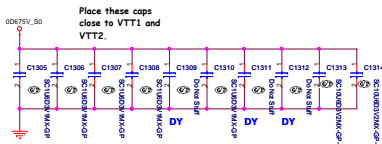
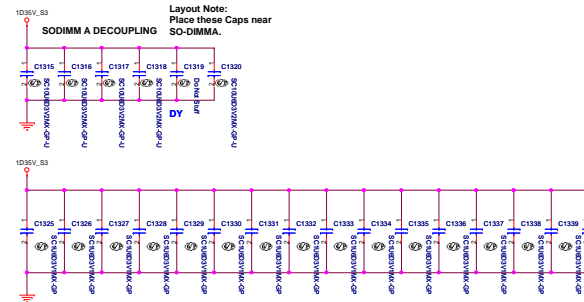
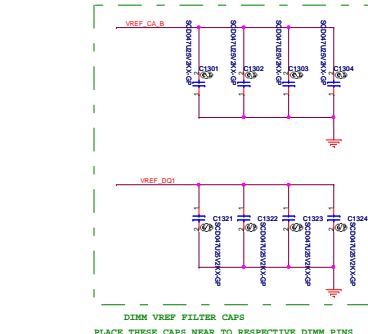
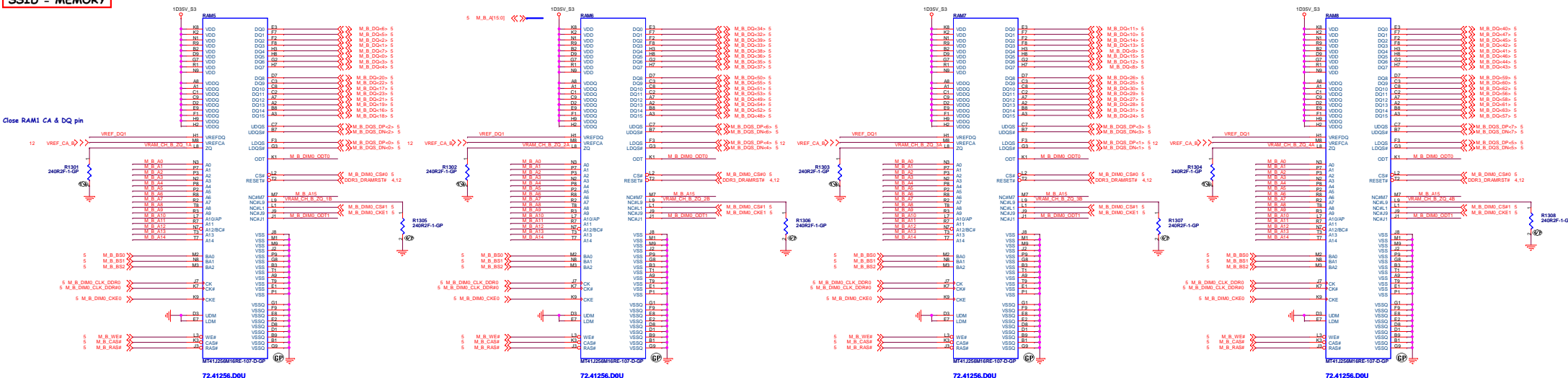


For Intel Recommend Close to DIMM

For Intel Recommend Close to DIMM

SSID = MEMORY

Close RAM1 CA & DQ pin



5

4

3

2

1

D

D

C

C

(Blanking)

B

B

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A

A

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Title SODIMM3_SODIMM4 (Reserved)

Size A4	Document Number Storm 2	Rev -1
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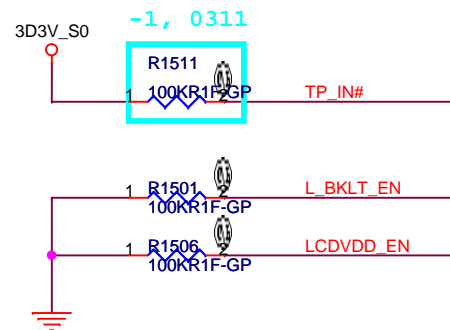
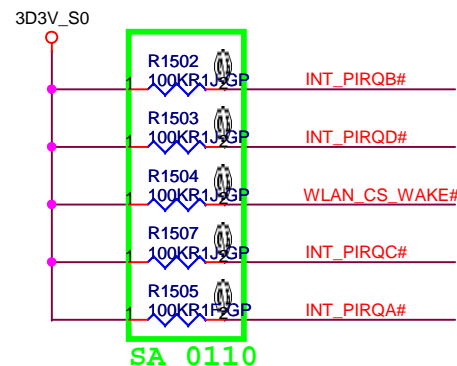
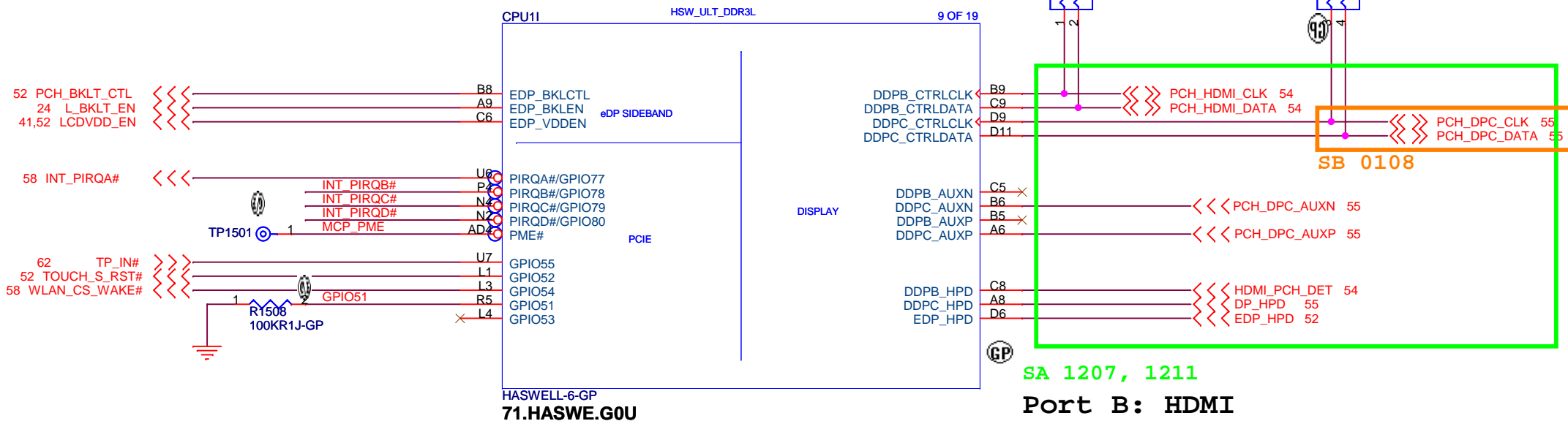
4

3

2

1

SSID = PCH



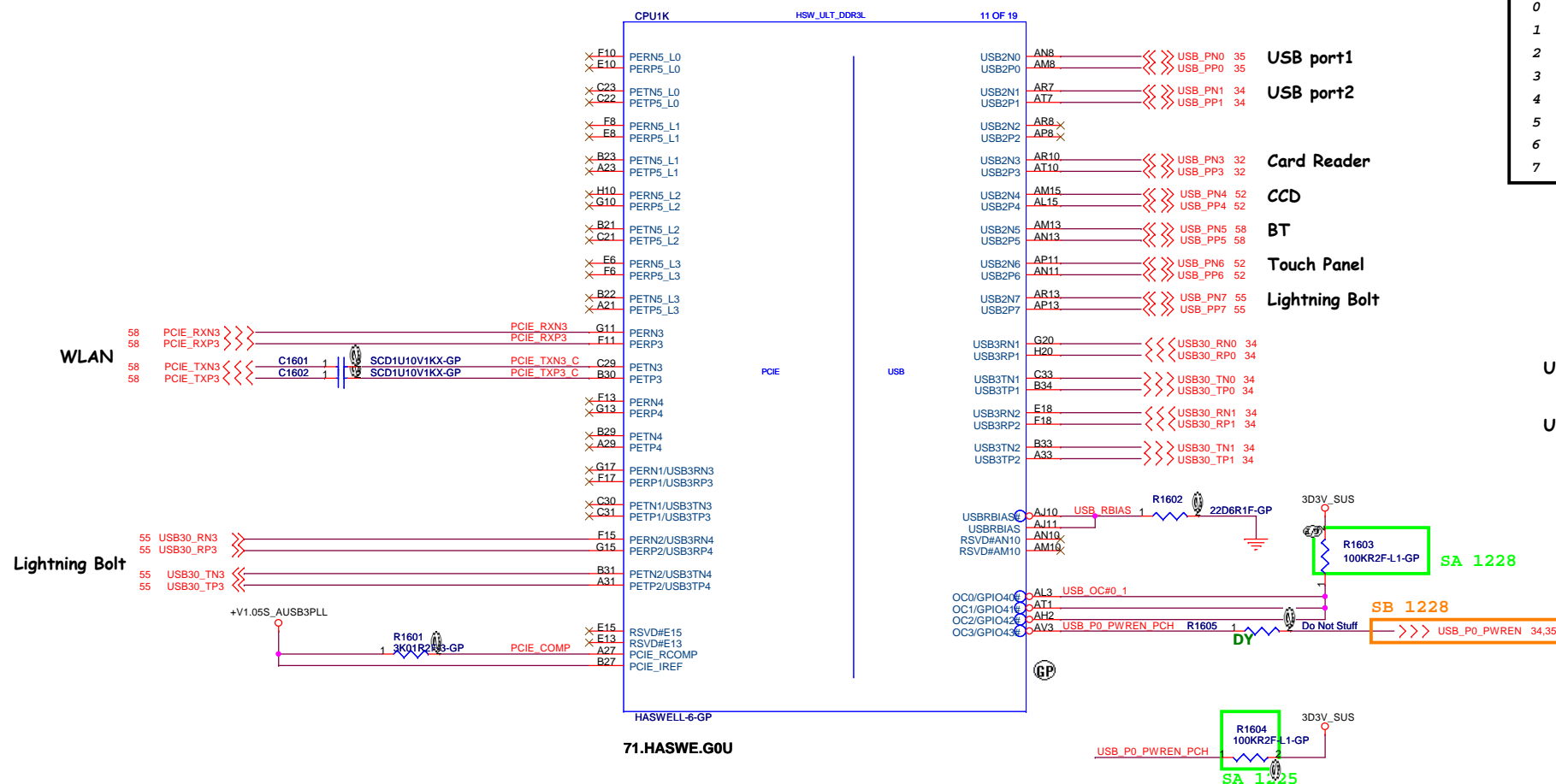
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Title PCH (DDI)		
Size A4	Document Number Storm 2	Rev -1
Date: Tuesday, April 02, 2013 Sheet 15 of 102		

SSID = PCH

USB Table

Pair	Device
0	USB3.0 Port 1
1	USB3.0 Port 2
2	NA
3	Card Reader
4	CCD
5	BT
6	Touch Panel
7	Lightning Bolt



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Title

CPU (PCI/USB)

Size

Document Number

Storm 2

A3

Segment Number

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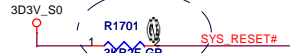
Rev

Rev
-1

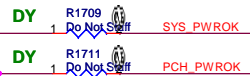
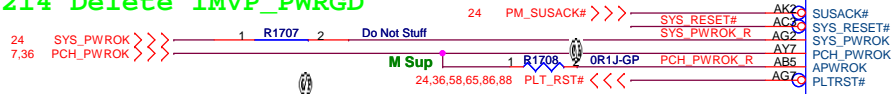
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SSID = PCH

Follow Intel CRB



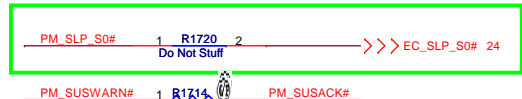
SA 1214 Delete IMVP_PWRGD



SB 0206



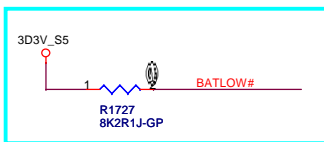
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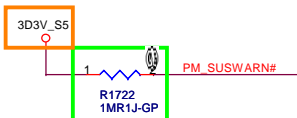
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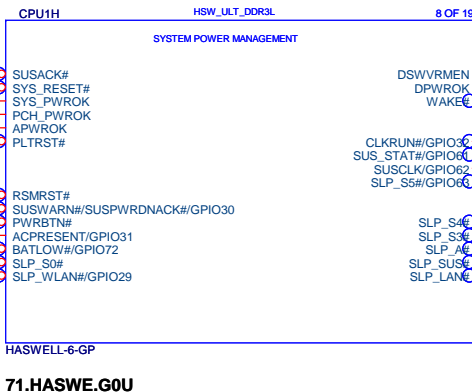
-1, 0318, for rearming from DSx



SB 1228



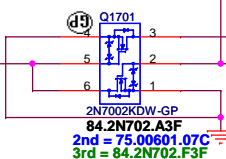
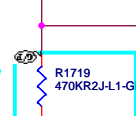
SA 1225



71.HASWE.G0U

Non DS3

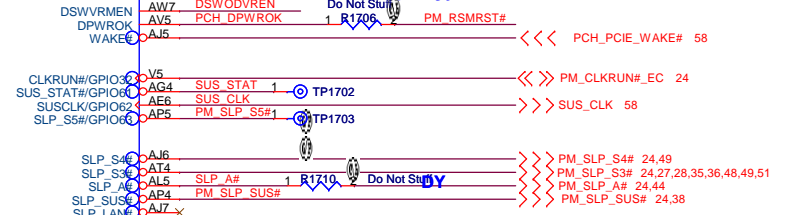
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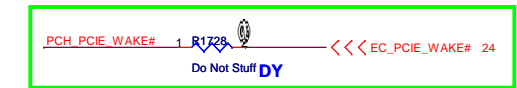
84.2N702.A3F
2nd = 75.00601.07C
3rd = 84.2N702.F3F

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

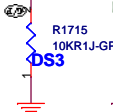
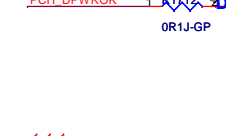
Non DS3



SA 1220

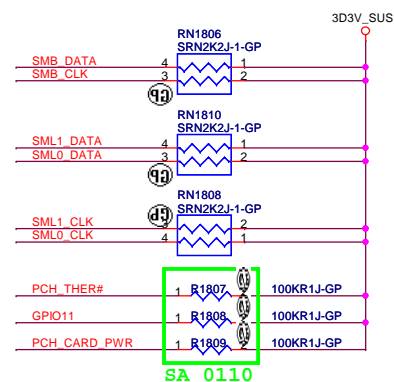
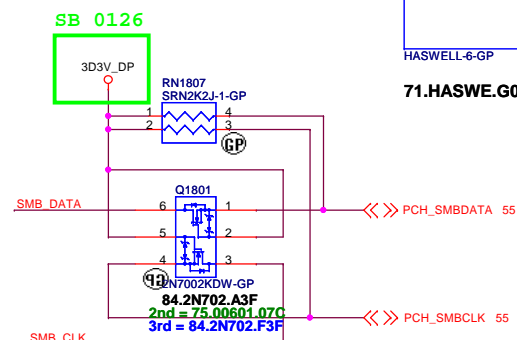
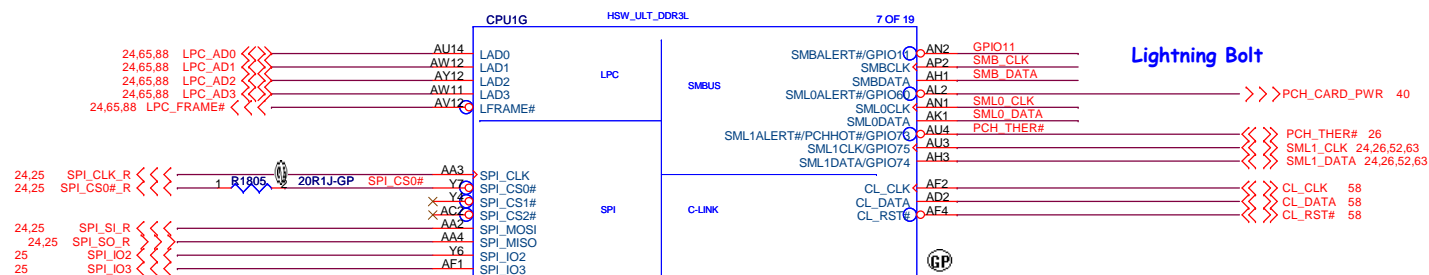
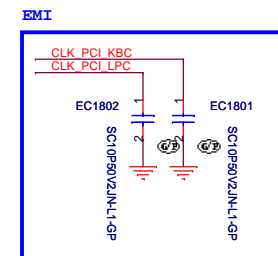
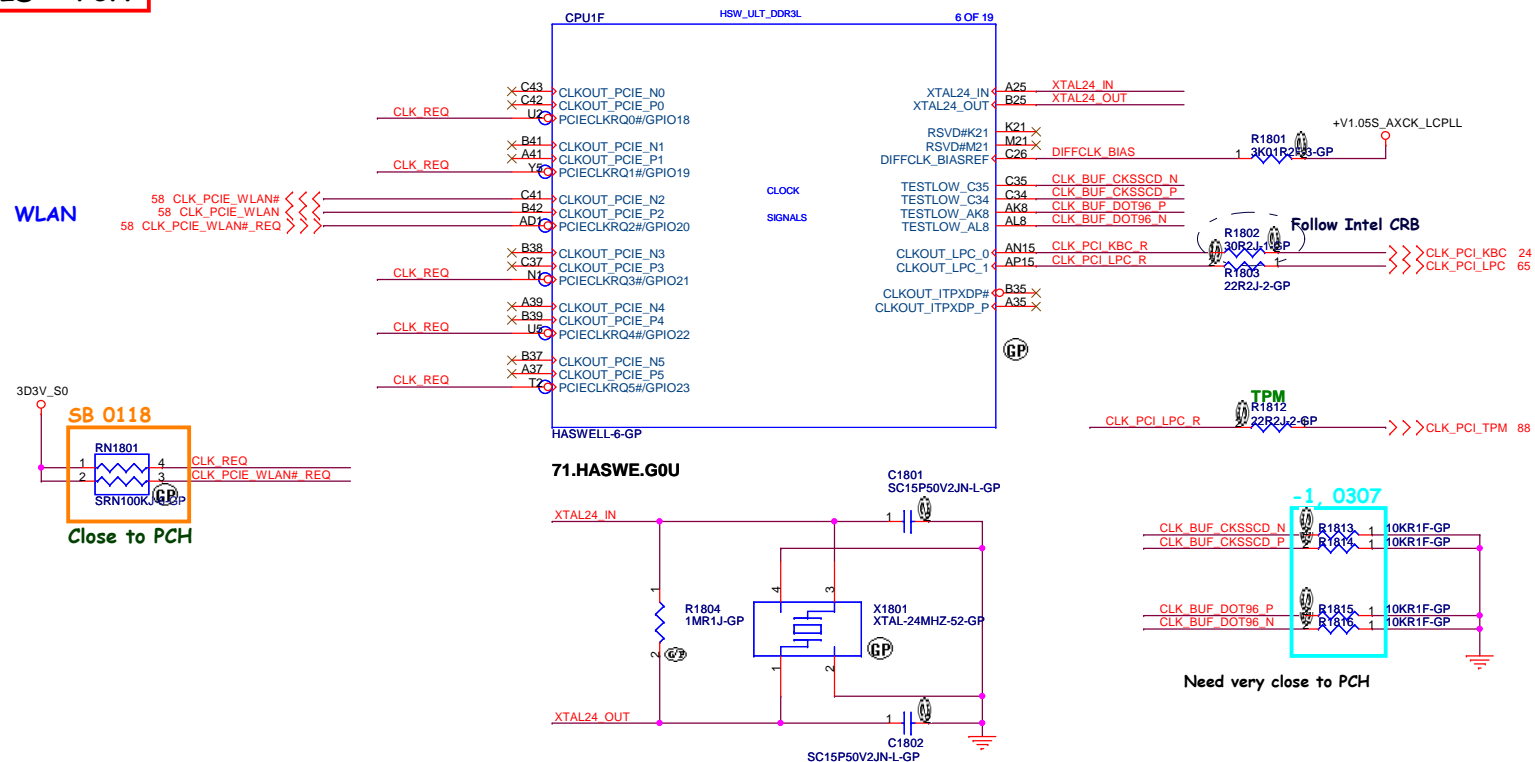


PCH_DPWROK



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SSID = PCH



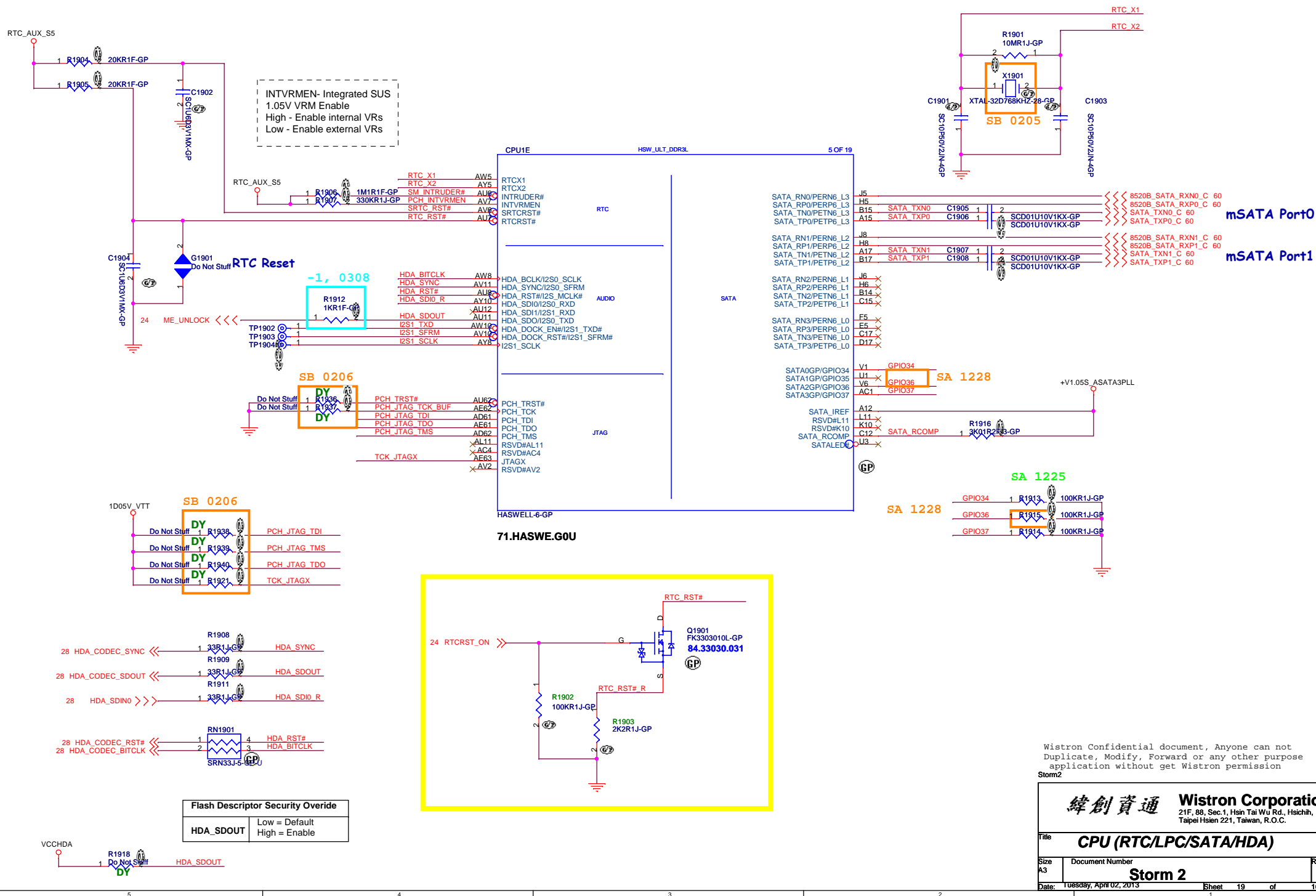
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Title	PCH (PCI-E/SMBUS/CLOCK/CL)
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SSID = PCH



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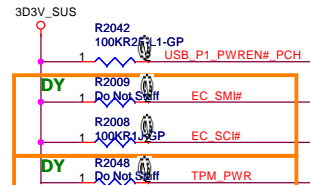
Title	CPU (RTC/LPC/SATA/HDA)
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SSID = PCH

SB 0223

-1, 0401



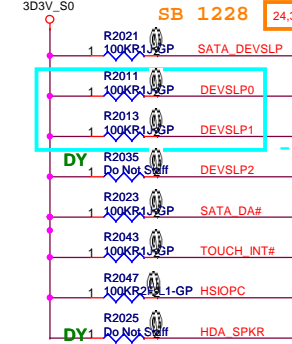
SA 1219

58 BT_CS_NOTICE <<<



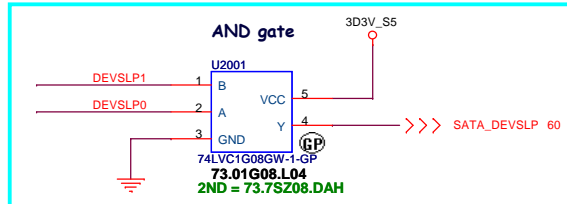
SB 1228

24,35 USB_P1_PWREN# <<<



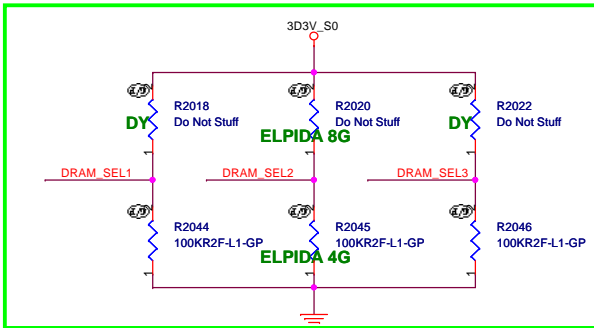
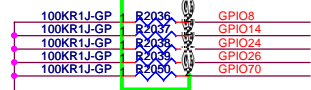
-1, 0314

-1, 0208, suggested by vender for RAID0



No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

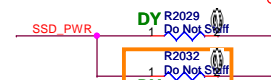
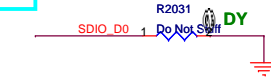
SA 0110



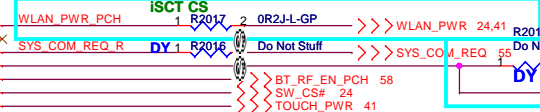
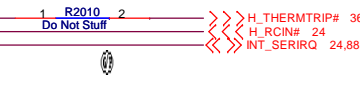
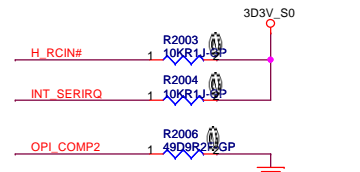
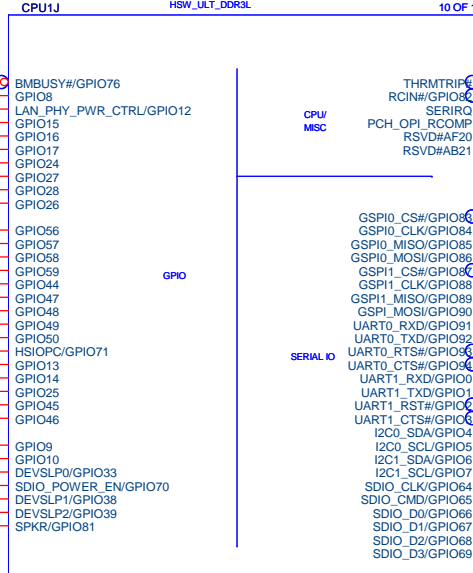
SA 1212 DRAM SEL

A16 SWAP OVERRIDE STRAP(SDIO_D0)	
STP_A16OVR	LOW = A16 SWAP OVERRIDE HIGH = NO OVERRIDE

GPIO91 DRAM_SEL1 Dual/Single channel	GPIO92 DRAM_SEL2	GPIO93 DRAM_SEL3	Status
0	0	0	ELPIDA 4G (Dual)
0	0	1	Hynix 4G (Dual 1Rx16)
0	1	0	ELPIDA 8G (Dual)
0	1	1	Micron 8G (Dual)
1	0	0	
1	0	1	
1	1	0	ELPIDA 4G (Single)
1	1	1	

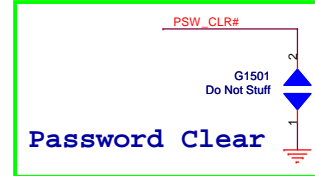


6SPI0_MOSI_BB50_R(SSD_PWR)	
PU	RESERVED
PD	SPI BUS



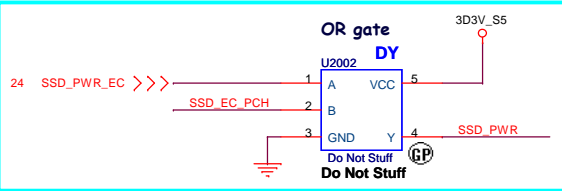
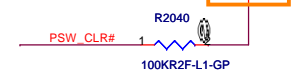
-1, 0312

-1, 0304



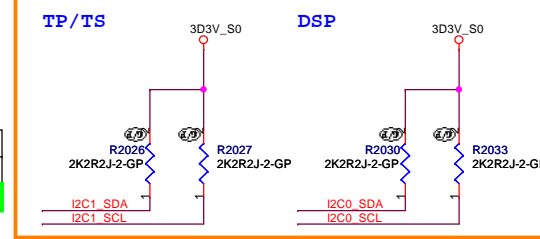
SA 1211

SB 0125



-1, 0304

SB 0125

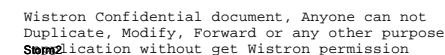


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PCH (GPIO)		
Title	Document Number	Rev
Size A3	Storm 2	-1
Date: Tuesday, April 02, 2013	Sheet 20 of 102	

1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling"](#) on page 532.

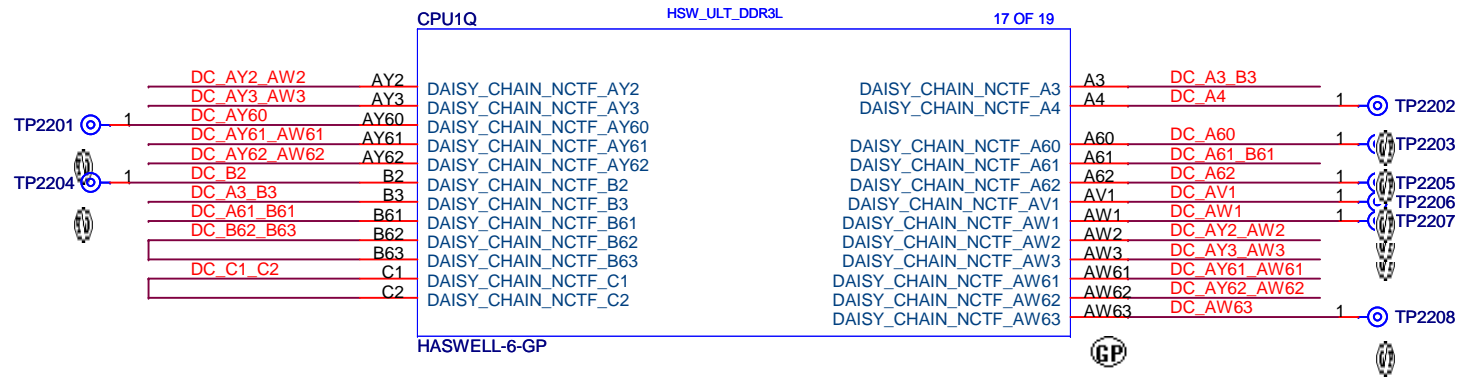


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Taipei Hsien 221, Taiwan, R.O.C.

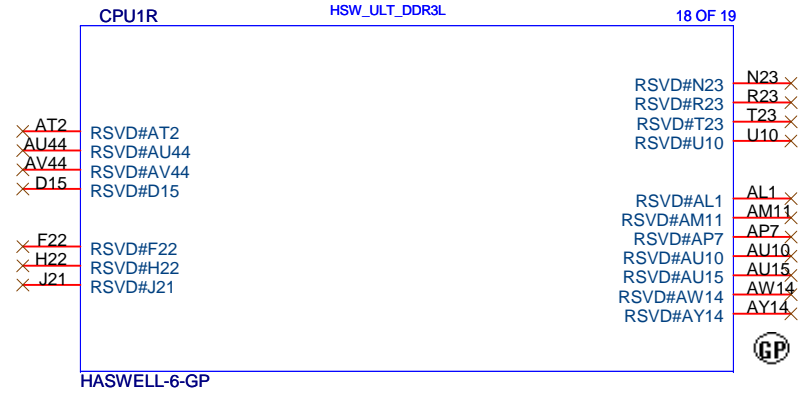
Title	CPU (POWER)
-------	--------------------

Size A3	Document Number Storm 2	Rev -1
Date:	Monday, March 18, 2013	Sheet 21 of 102

SSID = CPU



71.HASWE.G0U

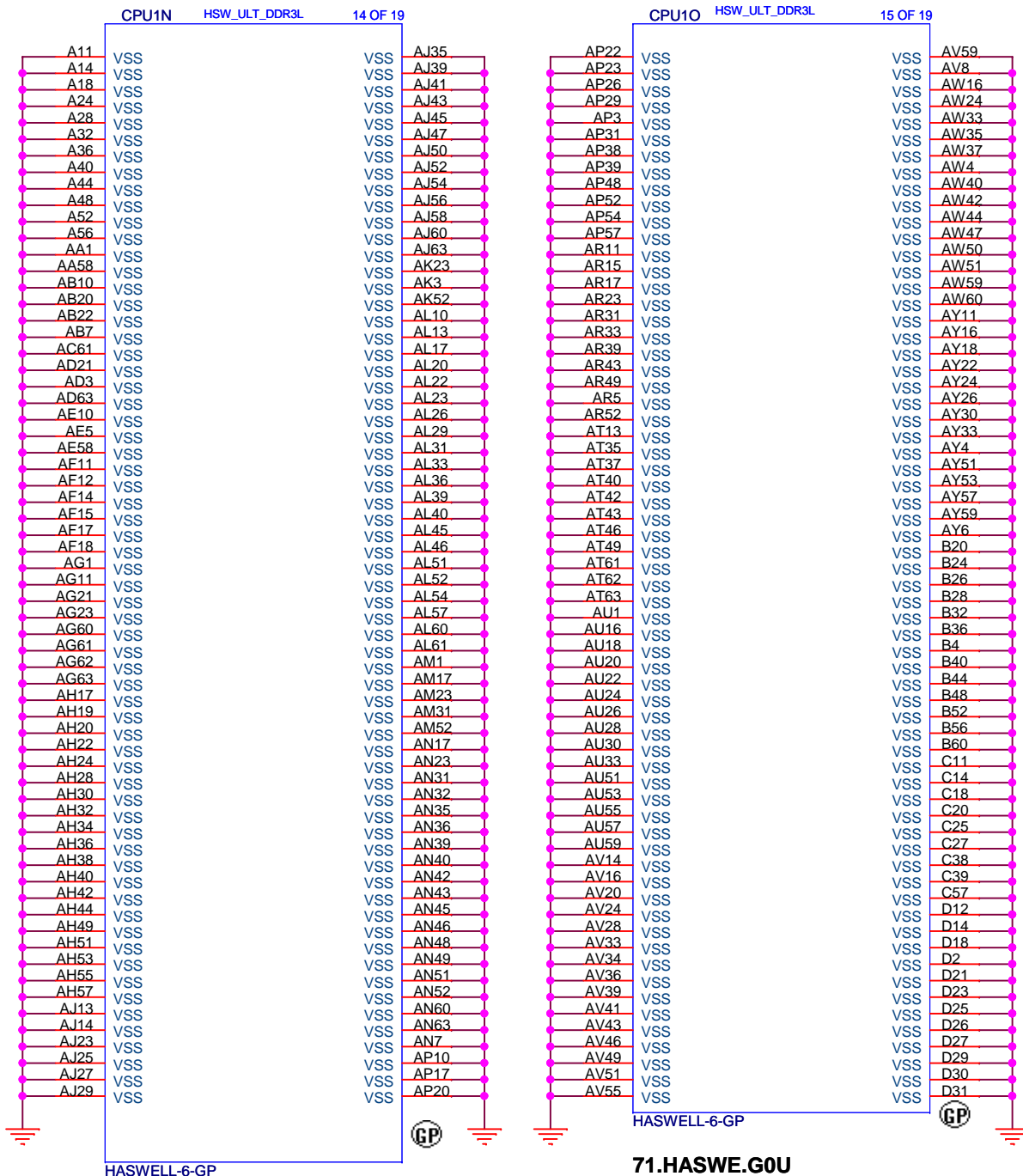


71.HASWE.G0U

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Title CPU (RSVD)			
Size A4	Document Number Storm 2	Rev -1	
Date: Friday, February 01, 2013	Sheet 22	of 102	

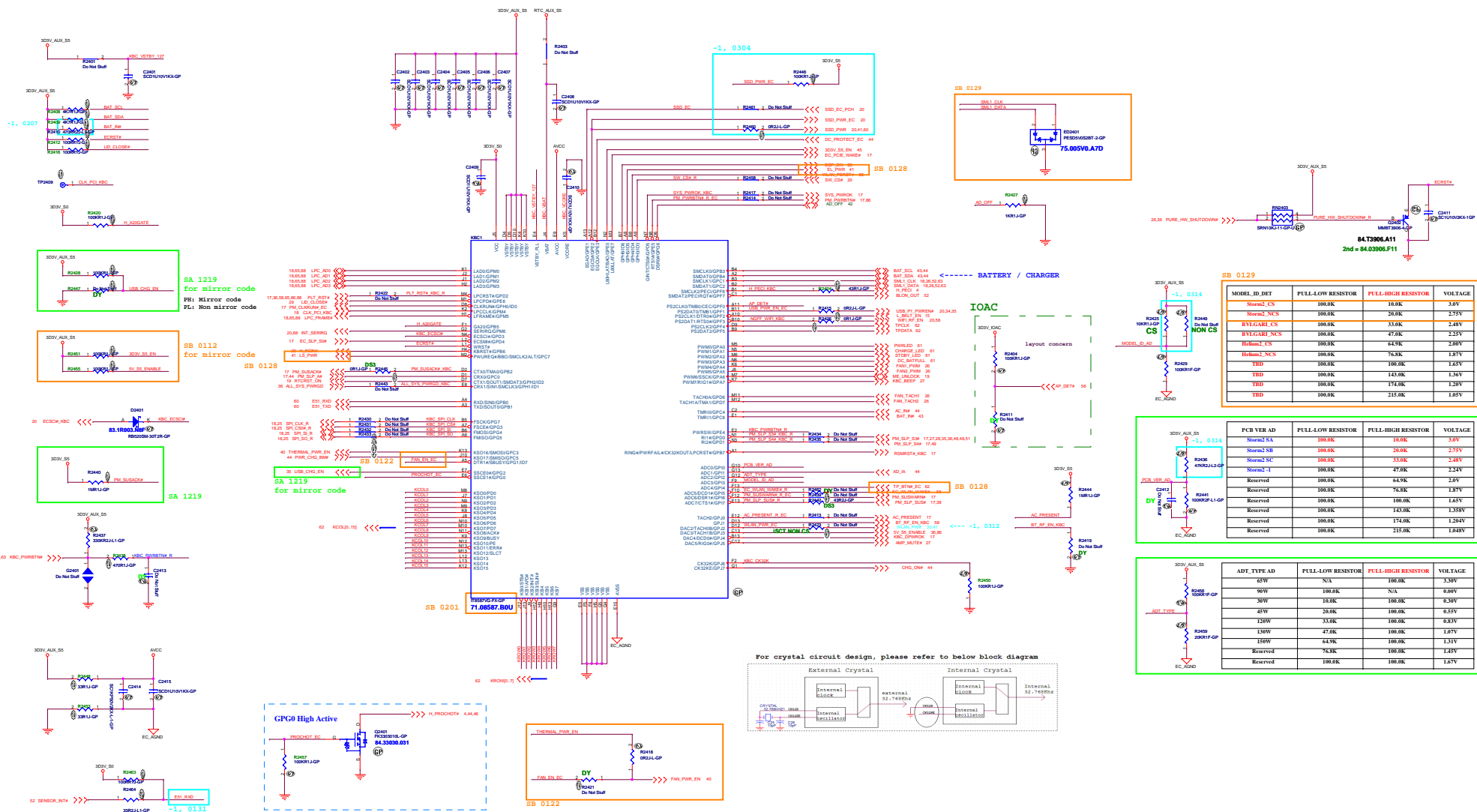
SSID = PCH



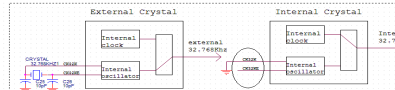
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Title		
PCH (VSS)		
Size	Document Number	Rev
A4	Storm 2	-1
Date	Friday, December 28, 2012	Sheet 23 of 102

SSID = KBC



For crystal circuit design, please refer to below block diagram



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50002

緯創資通

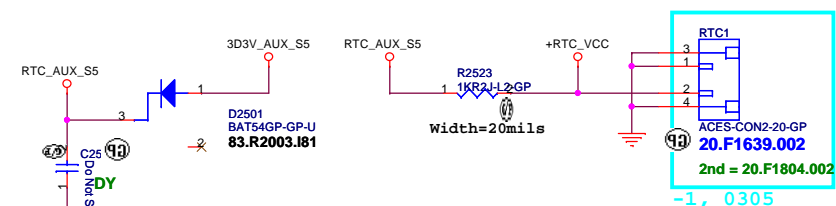
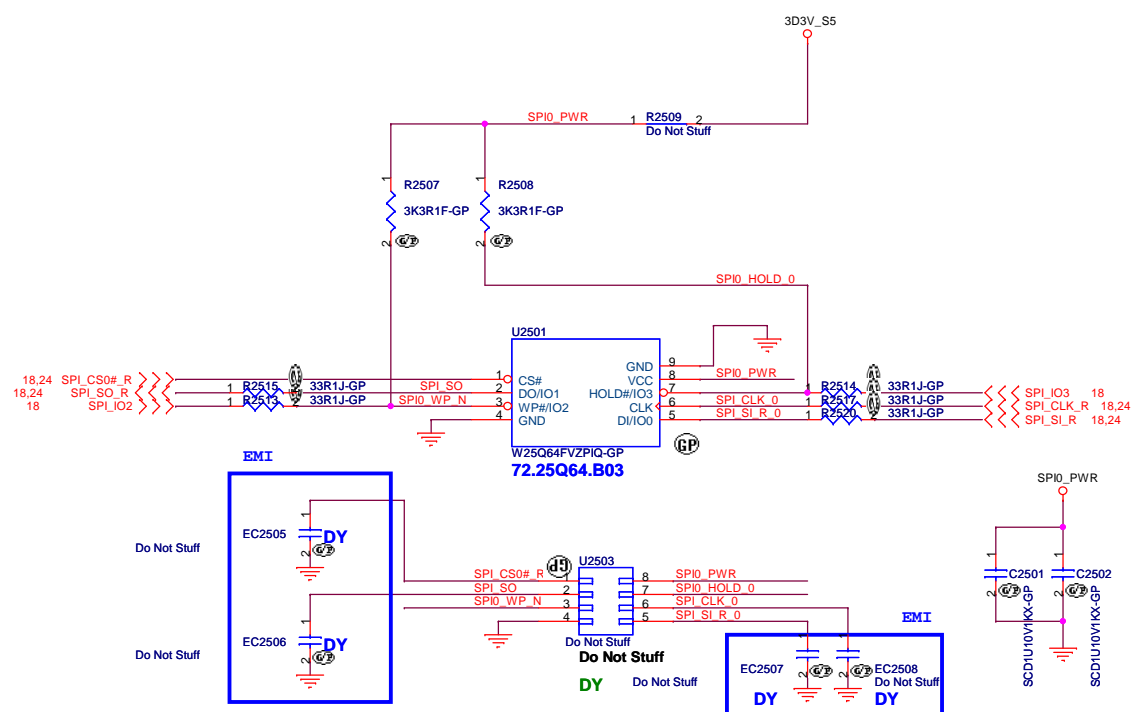
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu,
Taipei Hsein 301, Taiwan, R.O.C.

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH

SSID = RBAT

SPI ROM Equal length need to less than 500mil

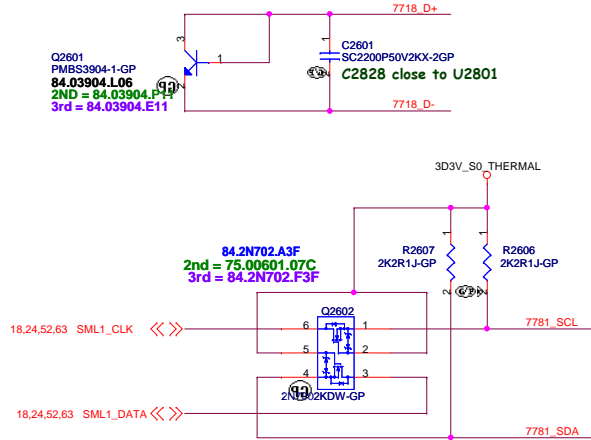


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Title			
Flash/RTC			
Size A3	Document Number		Rev
	Storm 2		-1
Date:	Tuesday, April 02, 2013	Sheet	25 of 102

SSID = Thermal



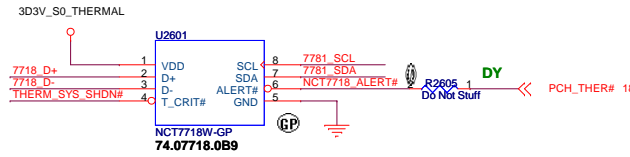
Layout notice :

- * Put the C1 2200pF to close the nct7718W
- * Add ground shielding for D+ and D- traces
- * D+/D- route has to be away from the high noise area
- * The recommended traces width and ground shielding spacing are 10mils

Setting 91°C

The default value is trapping after power up 100ms by different pull-up resistors of T_CRIT# and ALERT# pin:

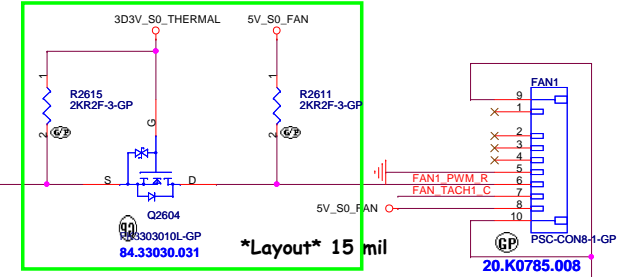
TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



Check!!!

SB 0128

SA 1222

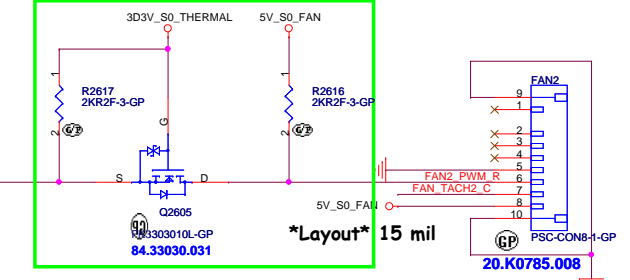


24 FAN1_PWM

24 FAN1_TACH1

24 FAN1_TACH2

SA 1222

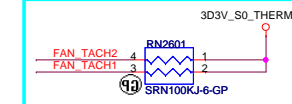


24 FAN2_PWM

24 FAN2_TACH1

24 FAN2_TACH2

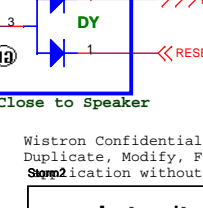
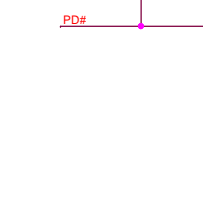
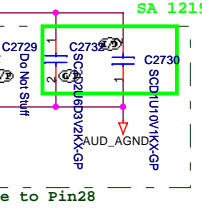
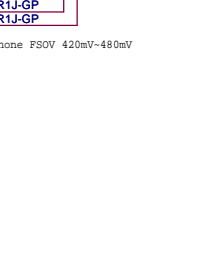
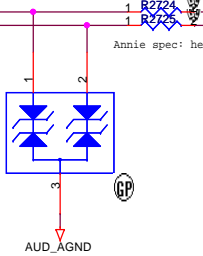
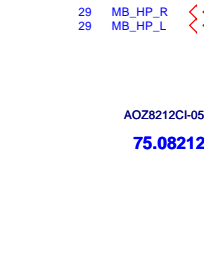
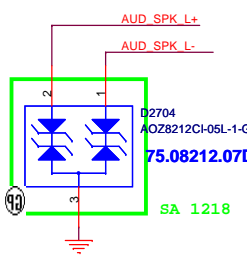
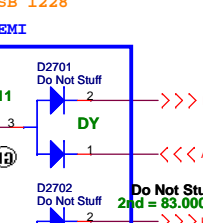
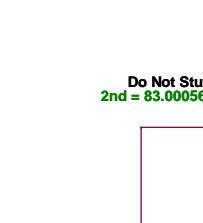
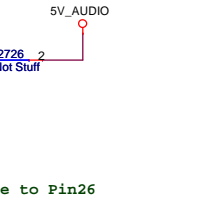
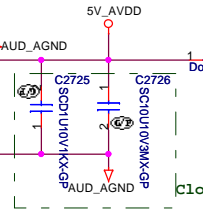
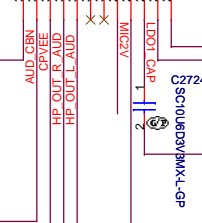
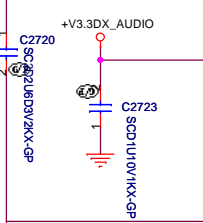
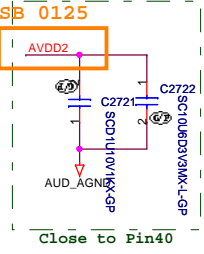
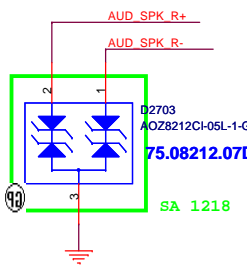
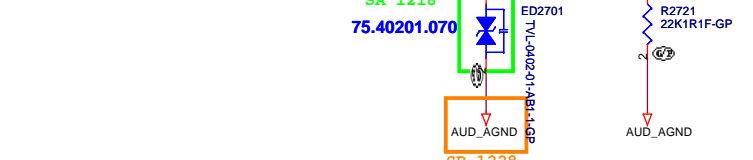
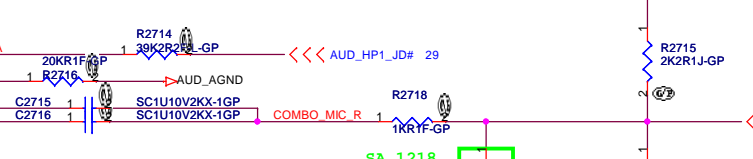
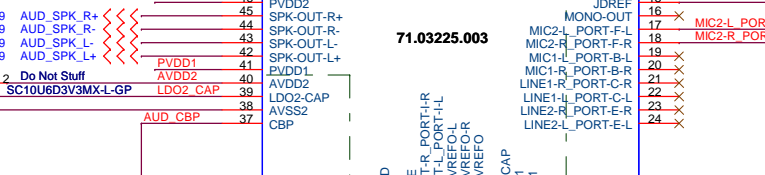
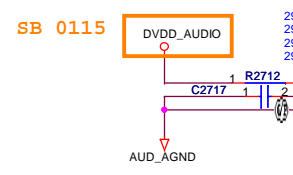
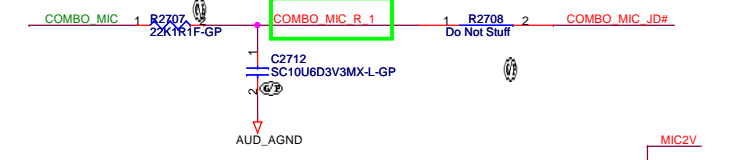
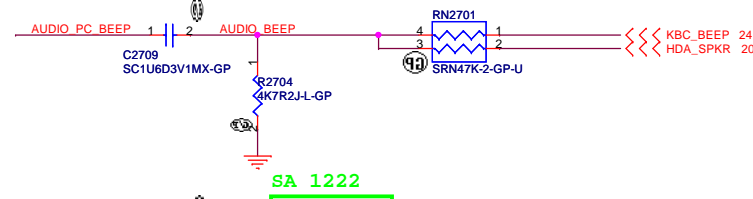
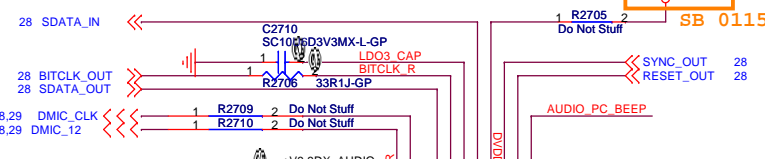
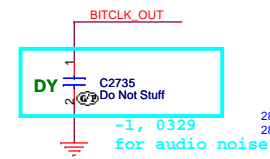
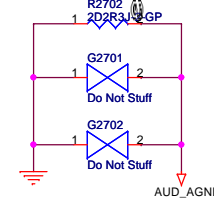
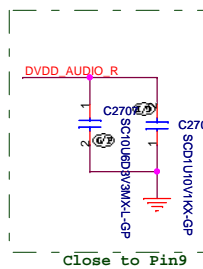
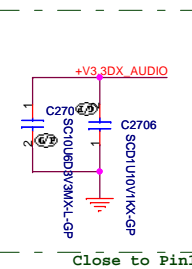
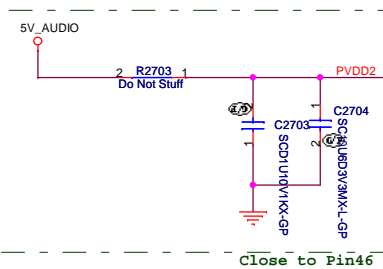
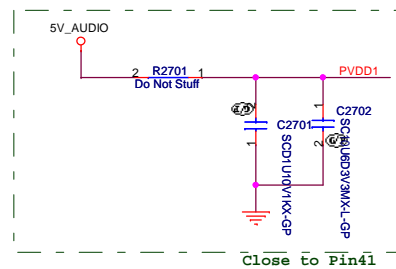
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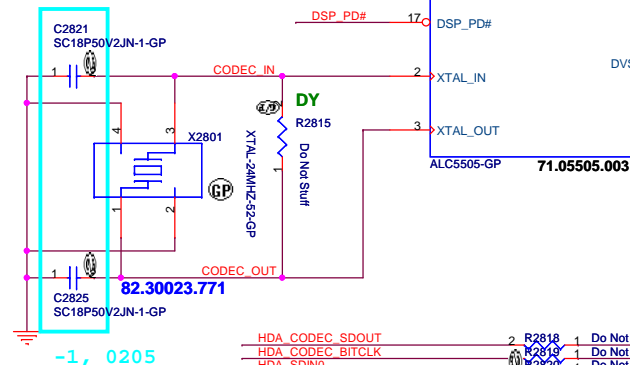
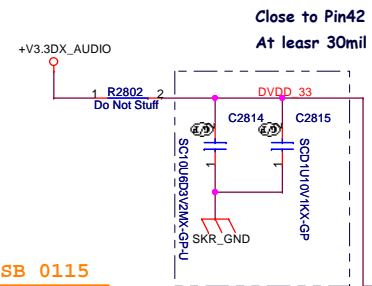
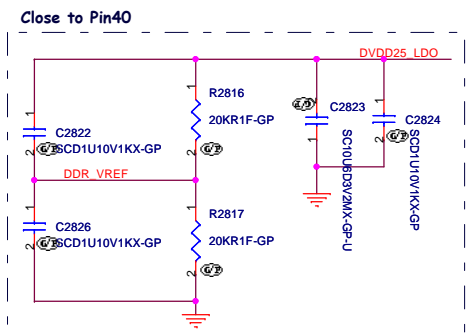
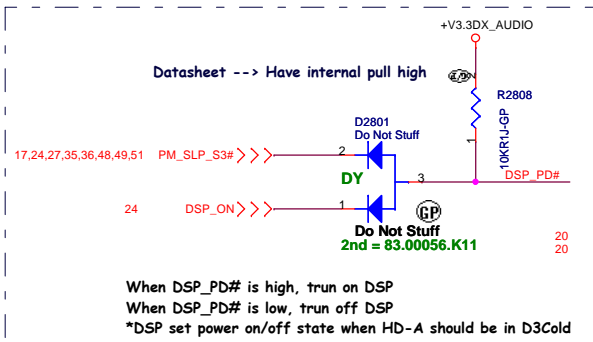
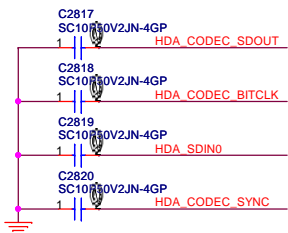
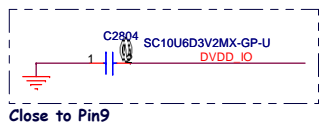


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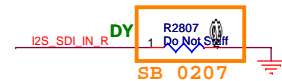
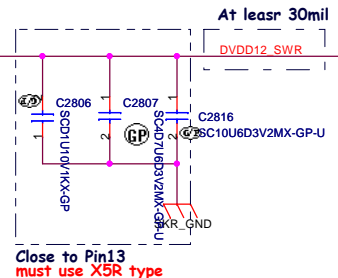
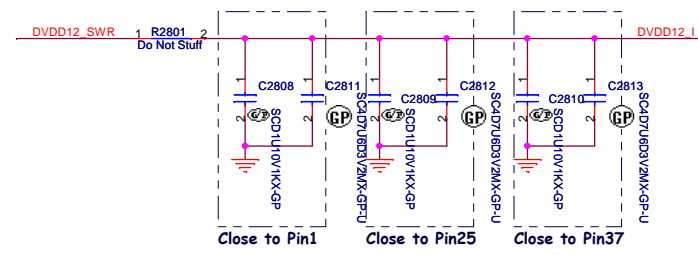
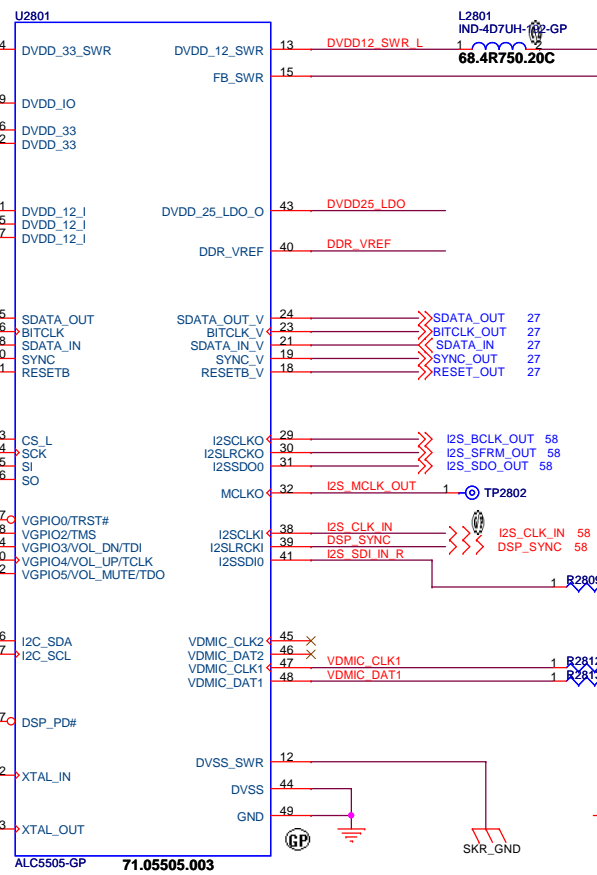
緯創資通 Wistron Corporation
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Title NUVOTON_NCT7718W
Size Custom Document Number Storm 2 Rev -1
Date: Monday, April 08, 2013 Sheet 26 of 102





- | | | | | | | |
|------------------|----|-------|---|--------------|----|------------|
| HDA_CODEC_SDOUT | 2 | R2818 | 1 | Do Not Stuff | DY | SDATA_OUT |
| HDA_CODEC_BITCLK | 19 | R2819 | 1 | Do Not Stuff | DY | BITCLK_OUT |
| HDA_CODEC_SYNC | 19 | R2820 | 1 | Do Not Stuff | DY | SDATA_IN |
| HDA_CODEC_RST# | 11 | R2821 | 1 | Do Not Stuff | DY | SDATA_IN |
| | | R2822 | 1 | Do Not Stuff | DY | SYNC_OUT |
| | | R2823 | 1 | Do Not Stuff | DY | RESET_OUT |



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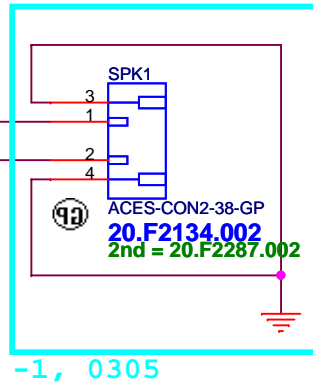
SSID = AUDIO

Speaker

27 AUD_SPK_L- >>>
27 AUD_SPK_L+ >>>

Layout Note:

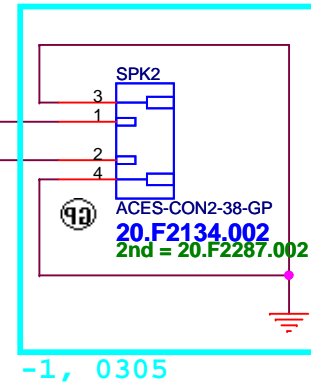
Trace width=40mil



27 AUD_SPK_R- >>>
27 AUD_SPK_R+ >>>

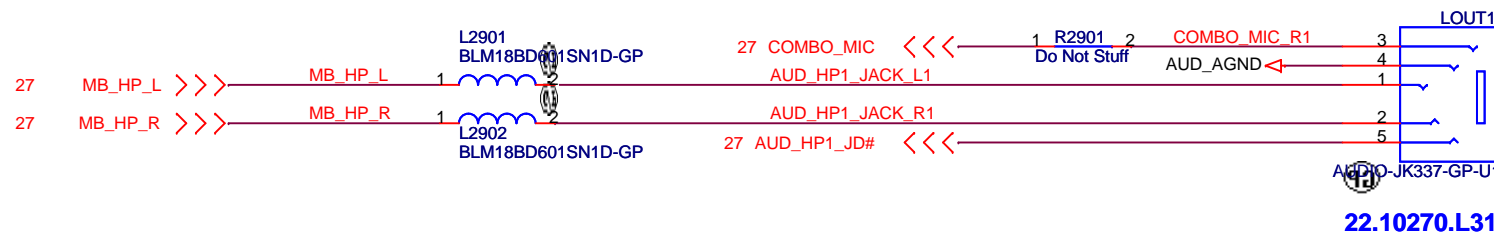
Layout Note:

Trace width=40mil

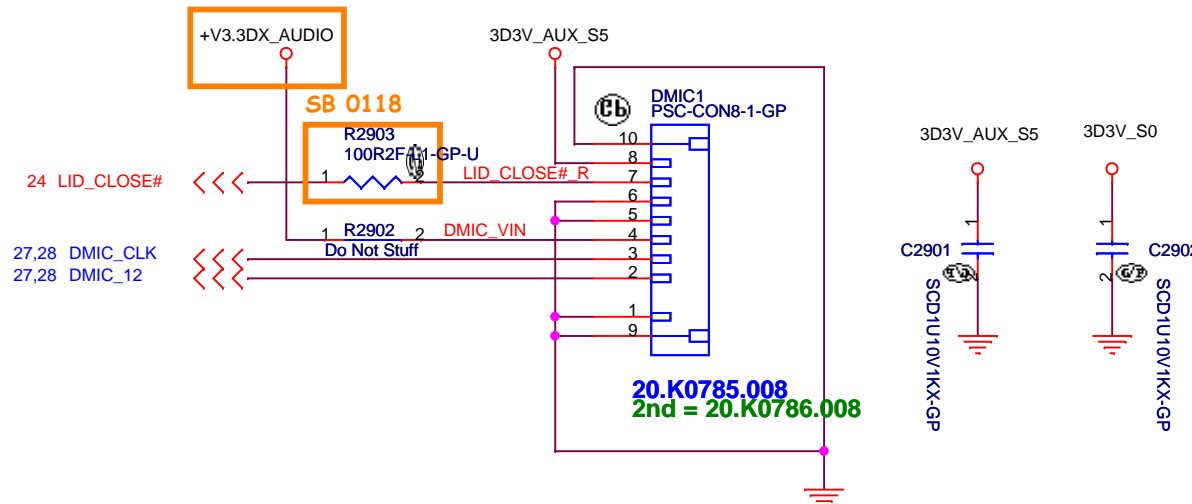


Combo Jack

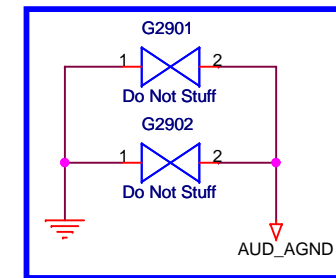
600ohm 100MHz
200mA 0.5ohm DC



DMIC & Hall Sensor



EMI



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Storm2

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Taipei Hsien 221, Taiwan, R.O.C.

Title Audio Jack & Hall Sensor

Size A4	Document Number Storm 2	Rev -1
Date Tuesday, April 02, 2013	Sheet 29	of 102

SSID = User.Interface

(Blanking)

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Storm2

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Title **LAN (Reserved)**

Size A4	Document Number Storm 2	Rev -1
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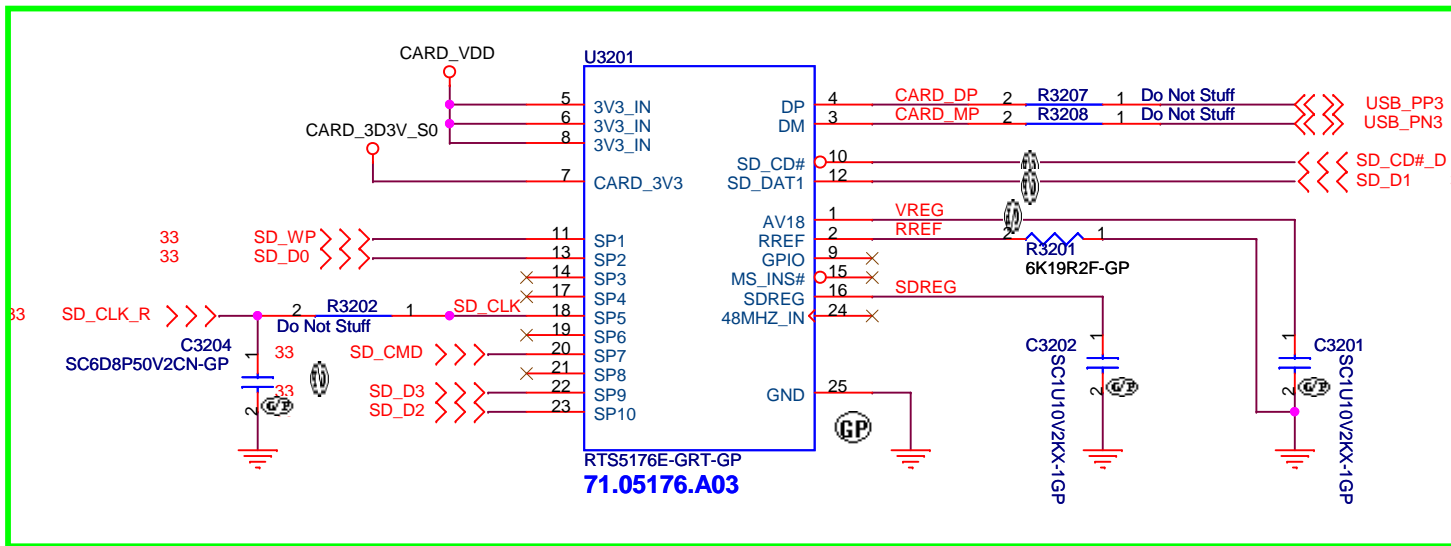
Date: Friday, December 28, 2012 Sheet 30 of 102

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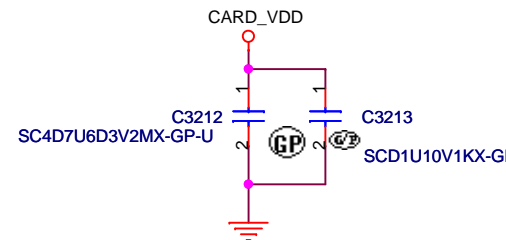
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Storm2

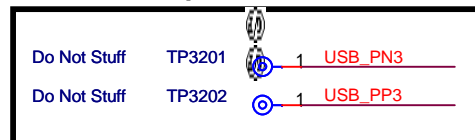
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Title RJ45 + Transformer (Reserved)			
Size A	Document Number Storm 2		Rev -1
Date: Friday, December 28, 2012		Sheet 31 of	102



SA 0104



FOR SIV,PLS near U3201



Pin#	Name	I/O Type	Description
1	AV18	O	Internal regulator for Analog blocks. An external capacitor should be connected
2	RREF	I	Connect external resistor (6.2K \pm 1%) to reference ground
3	DM	I/O	USB2.0 D- signal
4	DP	I/O	USB2.0 D+ signal
5	3V3_IN	I	3.3V power input
6	3V3_IN	I	3.3V power input
7	CARD_3V3	O	3.3V power supplied for all media cards
8	3V3_IN	I	3.3V power input
9	GPIO	I/O	General purpose input/output. Now it's used for LED blinking
10	SD_CD#	I	SD Card Detect pin
11	SP1	I/O	SD Write Protect pin and MS Data 1
12	SD_DAT1	I/O	SD/MMC Data 1
13	SP2	I/O	SD/MMC Data 0 and MS Data 5
14	SP3	I/O	MMC Data 7 and MS Data 4
15	MS_INS#	I	MS Card Detect pin
16	SDREG	O	Internal regulator for SD card. An external capacitor should be connected
17	SP4	I/O	MMC Data 6 and MS Data 0
18	SP5	I/O	SD/MMC Clock pin and MS Data 2
19	SP6	I/O	MMC Data 5 and MS Data 6
20	SP7	I/O	SD/MMC Command pin and MS Data 3
21	SP8	I/O	MMC Data 4 and MS Data 7
22	SP9	I/O	SD/MMC Data 3 and MS Clock pin
23	SP10	I/O	SD/MMC Data 2 and MS BS pin
24	48MHz_In	I	48MHz clock input
	Exposed PAD		The Exposed PAD must be connected to the reference ground

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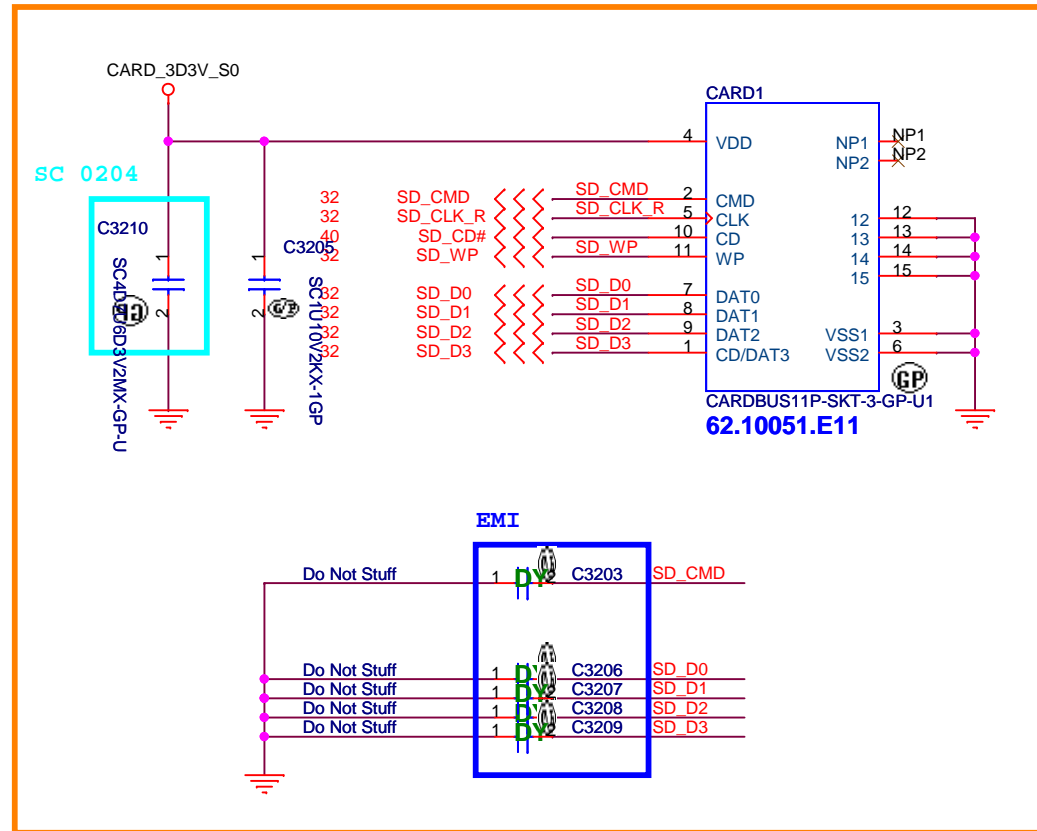
Title **CARD READER_RTS5176E**

Size A4 Document Number **Storm 2** Rev **-1**

Date: Tuesday, April 02, 2013 Sheet 32 of 102

SD Card Reader CONN.

SB 1228



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Title

CARD Reader CONN.

Size
A4

Document Number

Storm 2

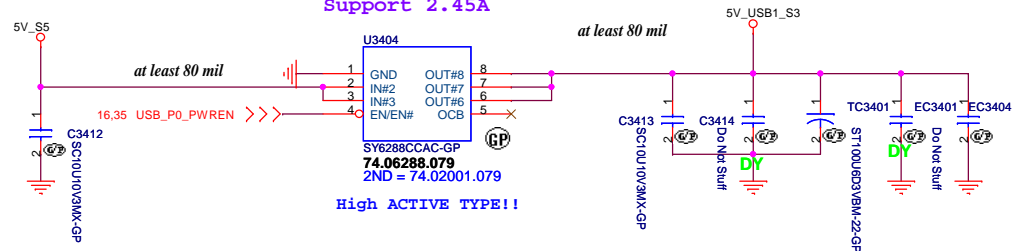
Rev
-1

Date: Tuesday, April 02, 2013

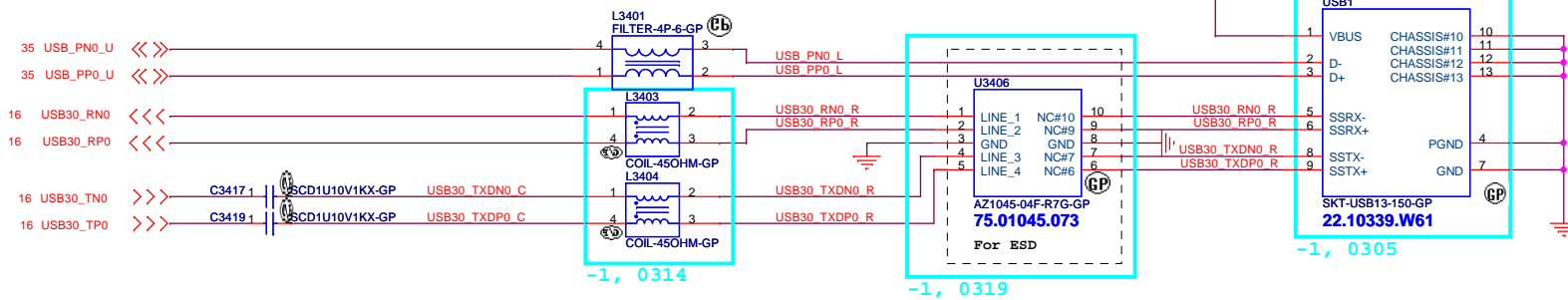
Sheet 33 of 102

SSID = USB

Change Main source
Support 2.45A



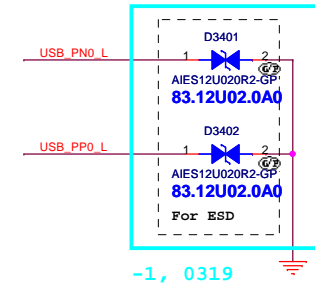
USB Charger Port
USB3.0 Port1



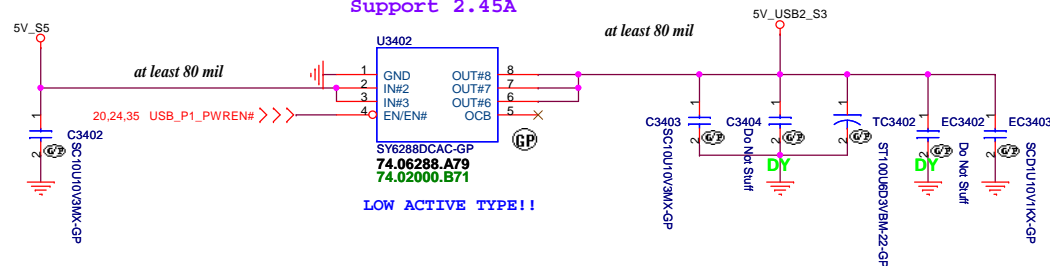
JE40 modify

USB 3.0 Connector
Pin definition

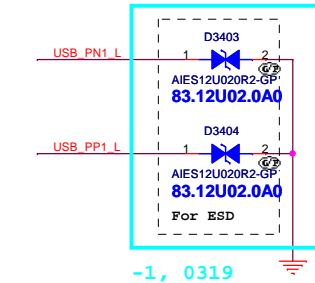
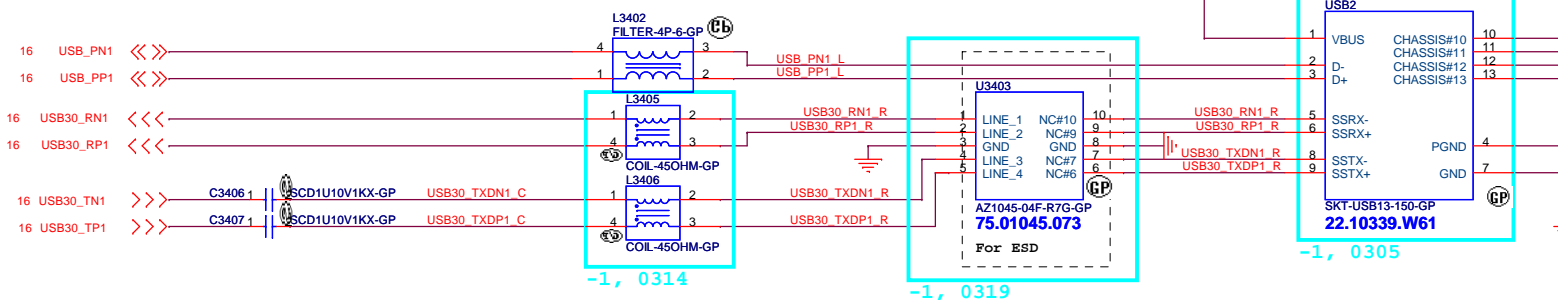
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX-
6	StdA_SSRX+
7	GND
8	StdA_SSTX-
9	StdA_SSTX+



Change Main source
Support 2.45A



USB3.0 Port2

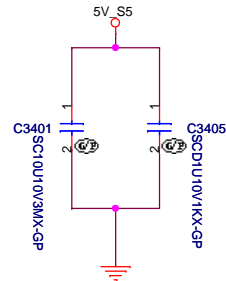


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Title	USB 3.0 Port	
Size A3	Document Number	Rev
	Storm 2	-1
Date: Tuesday, April 02, 2013	Sheet 34	of 102

USB Charger



Pin Description - SLG55583A

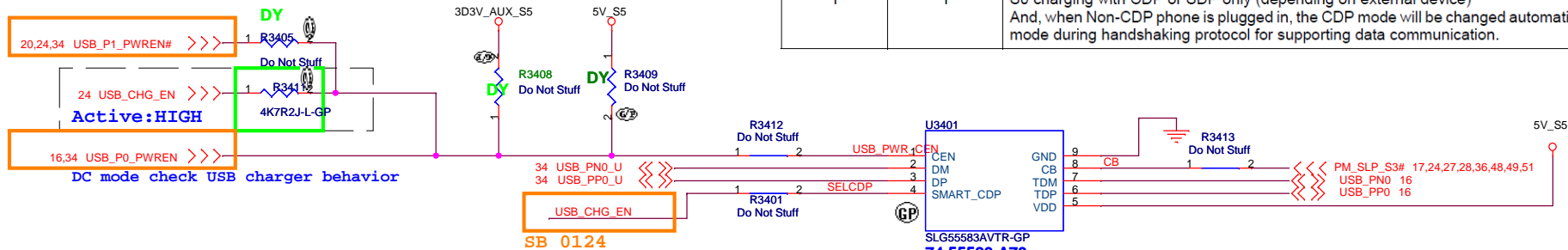
Pin Define

The symbol by pin number.

Pin #	Name	Type	Description
1	CEN	Output	N-FET Open Drain Output. Current Limit Switch (CLS) Control Output. CB changes from 0 to 1 or 1 to 0. CEN will be low for 2 seconds (typ)
2	DM	Input/Output	USB Connector D-
3	DP	Input/Output	USB Connector D+
4	SMART-CDP	Input	Input Control logic (see truth table)
5	VDD	PWR	Power Supply. Connect a 0.1μF capacitor between VDD and GND as close as possible to the device.
6	TDP	Input/Output	Host USB Transceiver D+ Connection
7	TDM	Input/Output	Host USB Transceiver D- Connection
8	CB	Input	Switch Control Bit 0 = autodetection charger identification active 1 = charging downstream port with active USB2.0 data communication mode with 1.5A support
9	Thermal Pad	GND	Ground

Truth Table

CB	SMART-CDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device) And, when Non-CDP phone is plugged in, the CDP mode will be changed automatically to SDP mode during handshaking protocol for supporting data communication.



SB 1228

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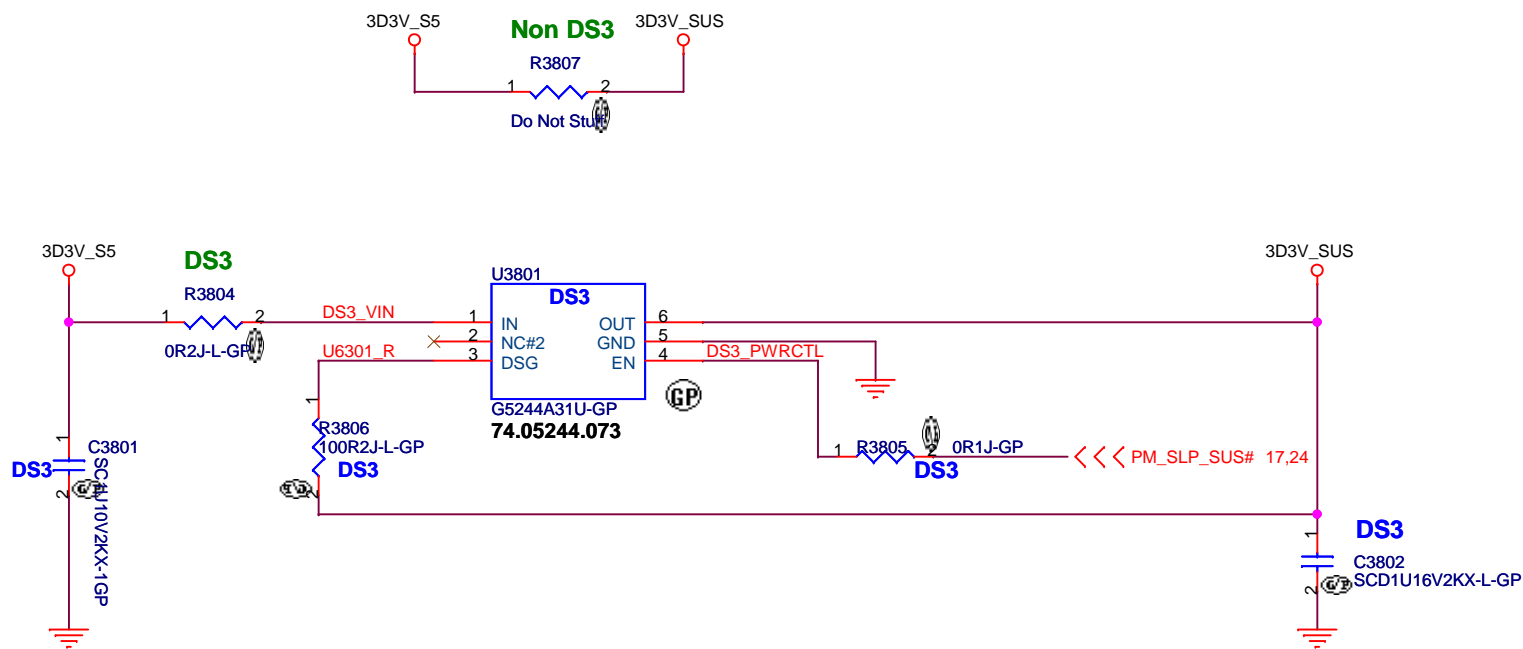
Title		
USB Charger (reserved)		
Size B	Document Number	Rev
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Date: Tuesday, April 02, 2013	Sheet 35 of 102	

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Title		
ADAPTER OCP / S3 reduction		
Size	Document Number	Rev
A4	Storm 2	-1
Date: Friday, December 28, 2012		Sheet 37 of 102



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Title

DS3

Size

Document Number

Rev

Storm 2

-1

Date

Tuesday, April 02, 2013

Sheet

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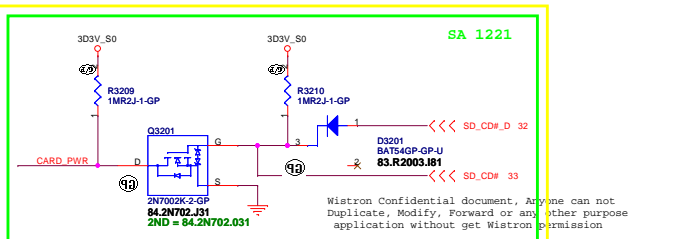
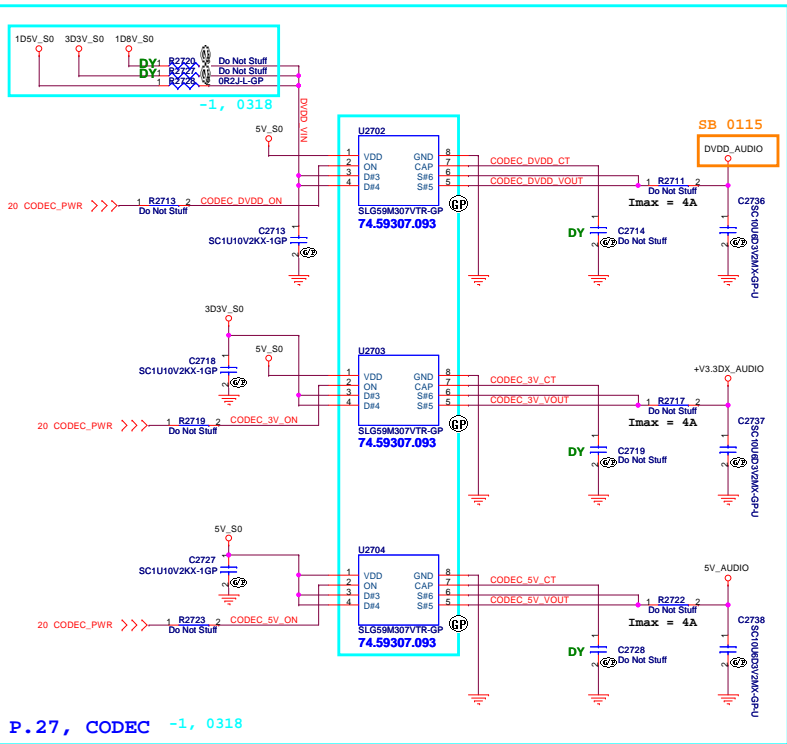
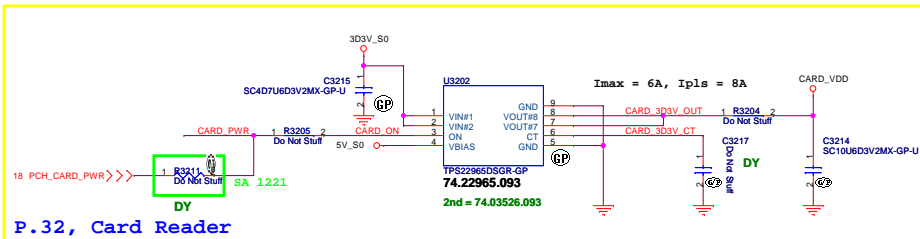
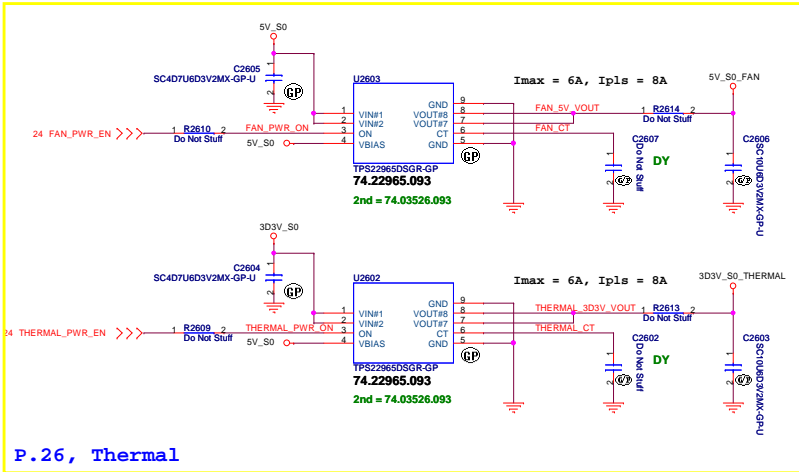
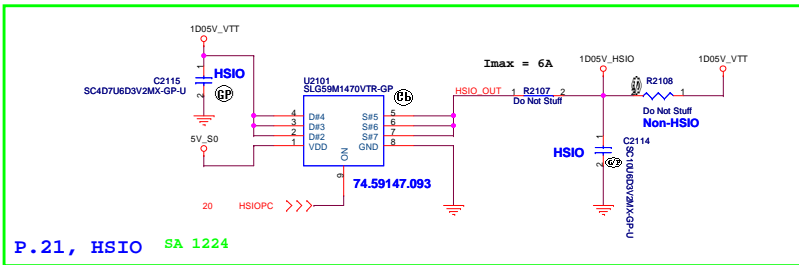
of

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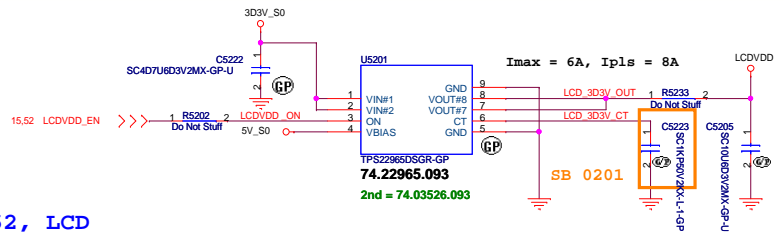
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Title			
1D05M (Reserved)			
Size A	Document Number		Rev
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Date:	Friday, December 28, 2012		Sheet 39 of 102

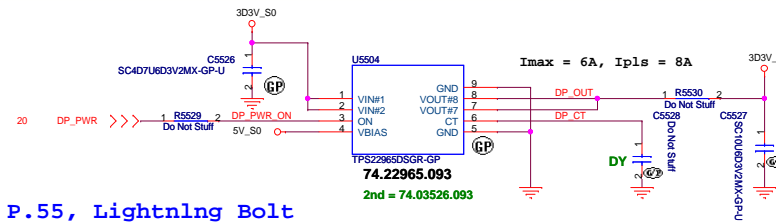


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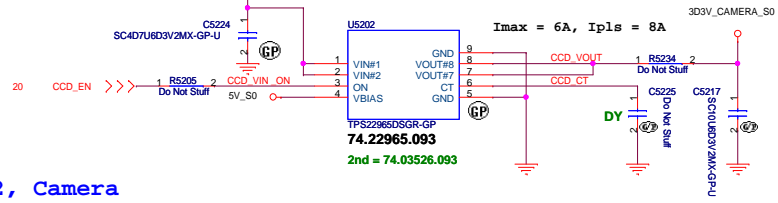
P.52, LCD



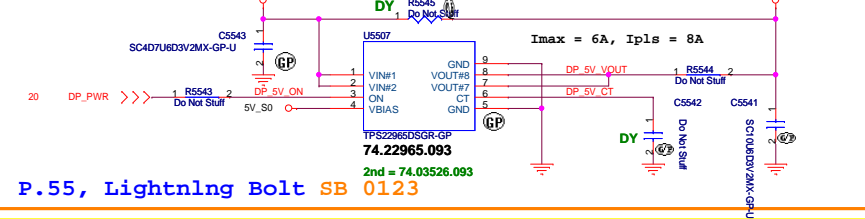
P.55, Lightning Bolt



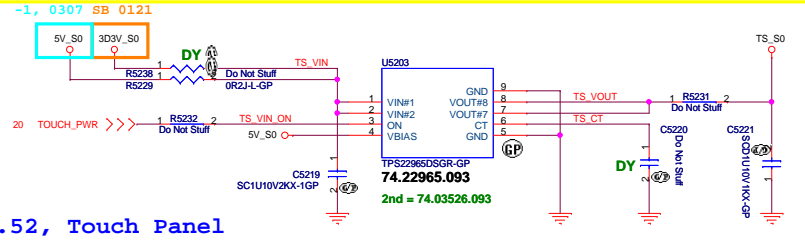
P.52, Camera



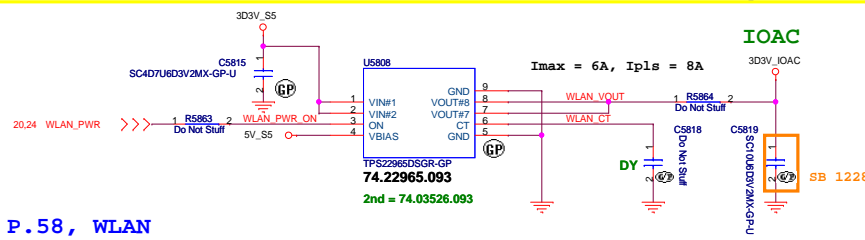
P.55, Lightning Bolt SB 0123



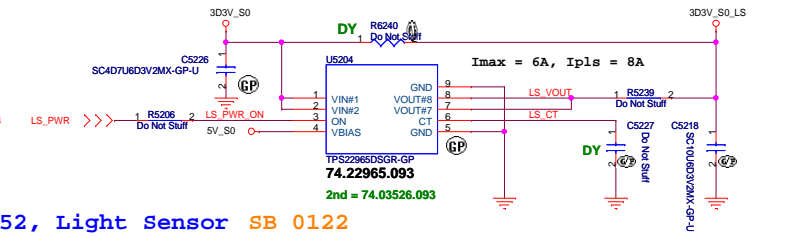
P.52, Touch Panel



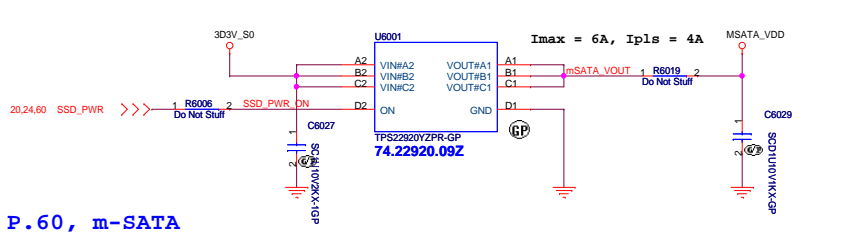
P.58, WLAN



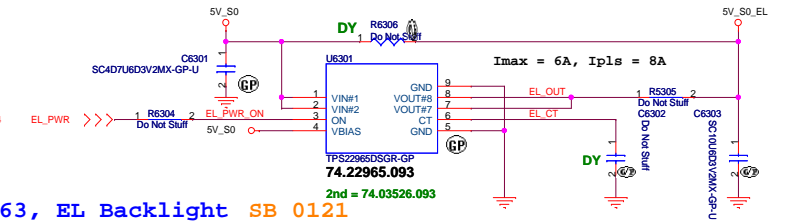
P.52, Light Sensor SB 0122



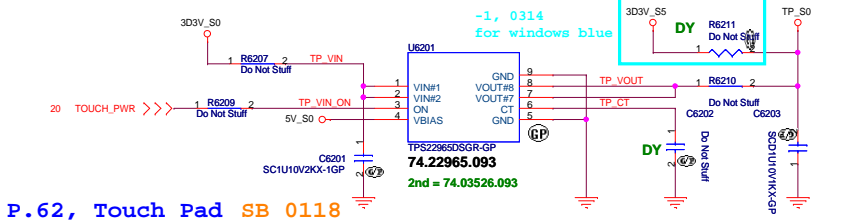
P.60, m-SATA



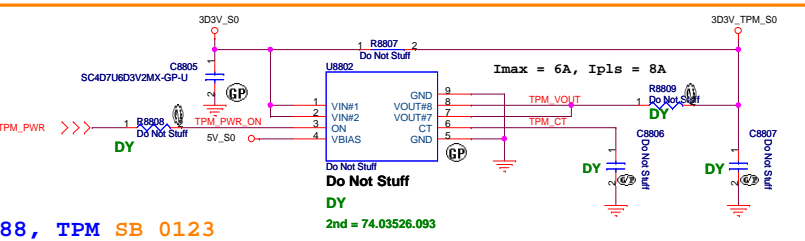
P.63, EL Backlight SB 0121



P.62, Touch Pad SB 0118



P.88, TPM SB 0123

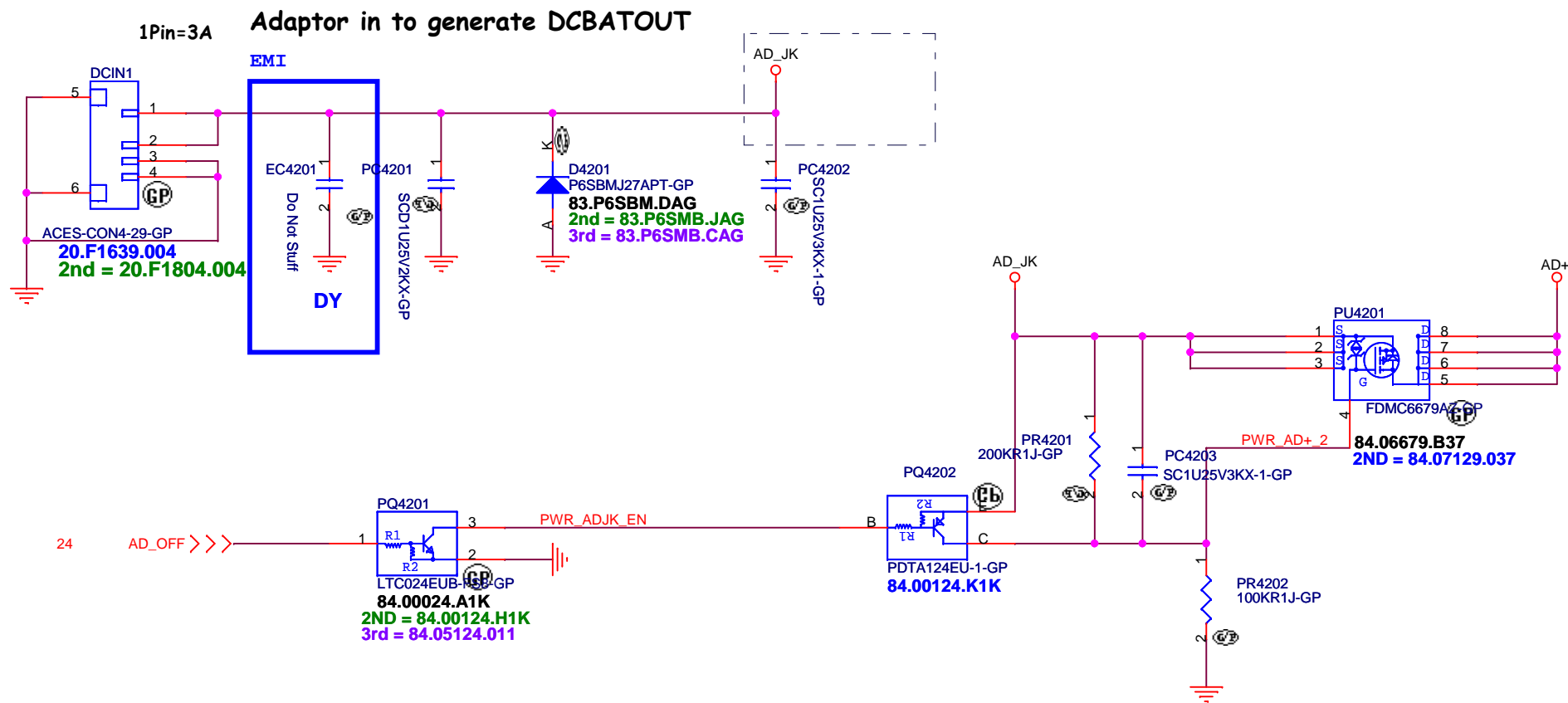


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Title		Connected Standby 2	
Size	Document Number	Rev	-1
Custom	Storm 2		
Date:	1/26/2013	Sheet	41 of 102

ANNIE solution



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Title

DCIN JACK

Size
A4

Document Number

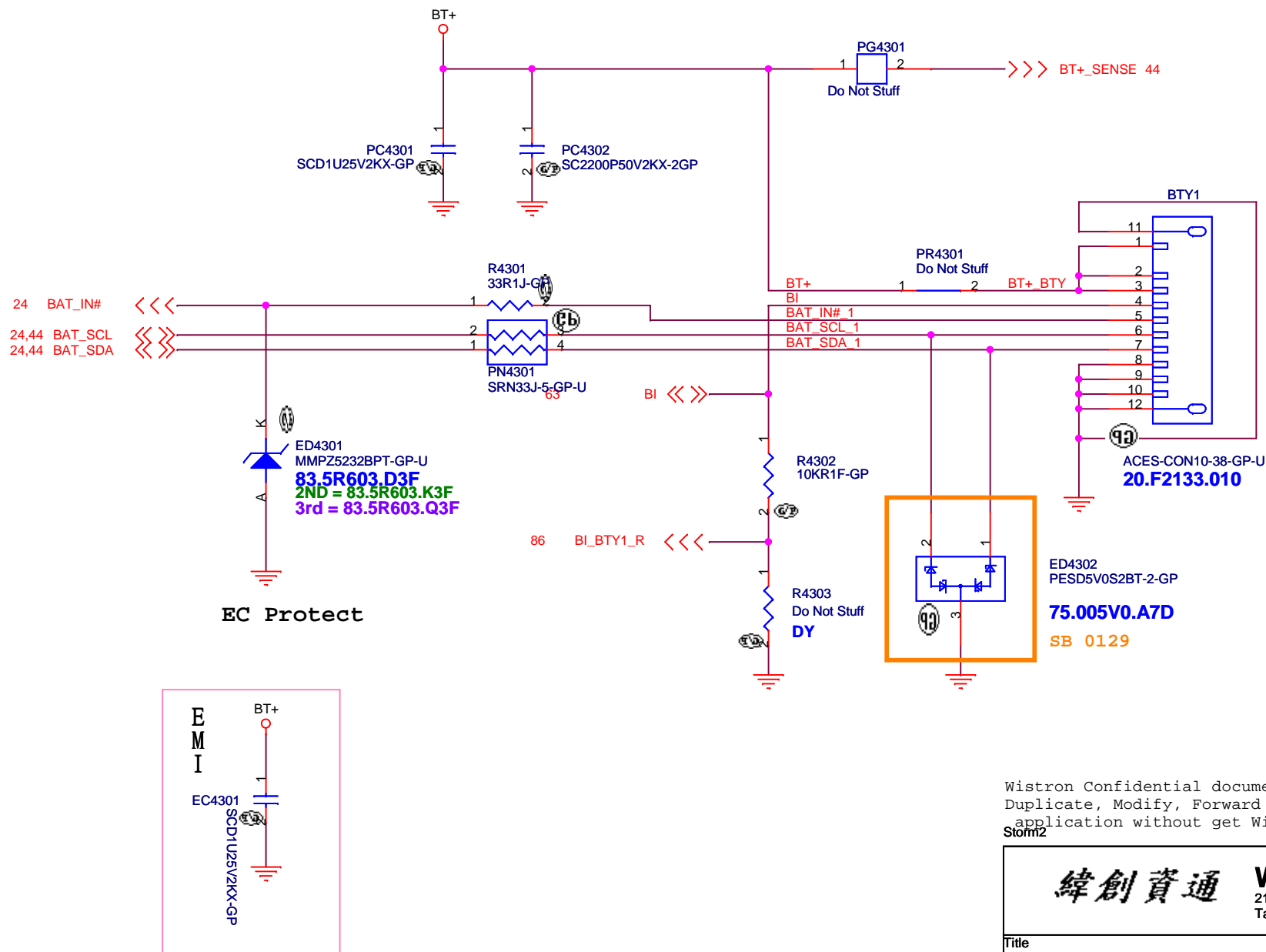
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Rev
-1

Date: Tuesday, April 02, 2013

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BATTERY CONNECTOR



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Title		
BATT CONN		
Size	Document Number	Rev
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Date	Tuesday, April 02, 2013	Sheet 43 of 102

AD+ total power	R1	R2
45w	56K	100K
65w	106K	100K

[illegible][illegible]

AC adapter detect current :

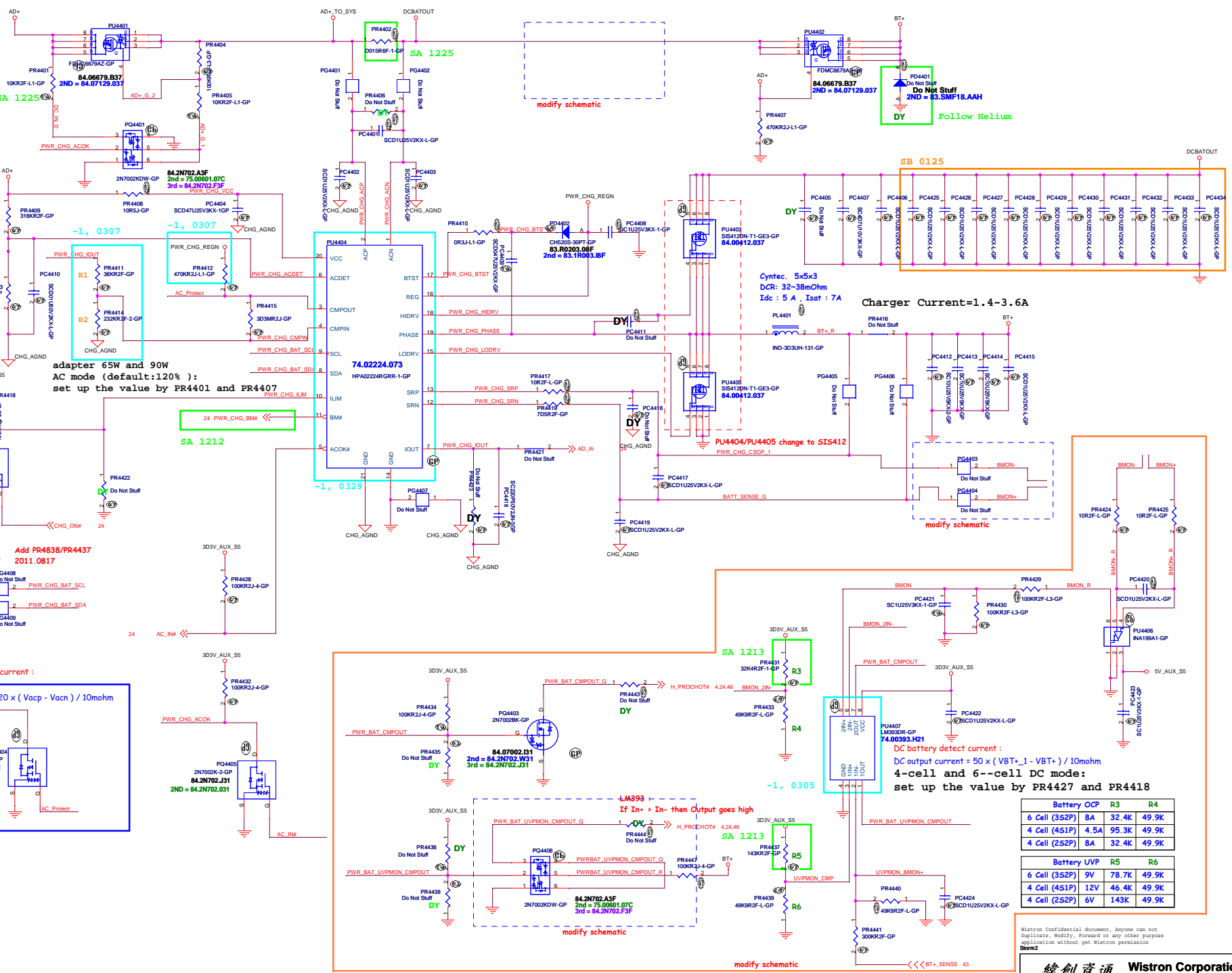
Ac input current = $20 \times (V_{acp} - V_{acn}) / 10\text{mohm}$

4.24,46 H_PRODCHOTA <<

check !!

PO4404
2N7002K-GP
84.2N702.J31
2ND = 84.2N702.031

AC_Protect



Battery	OCV	R3	R4
6 Cell (3S2P)	8A	32.4K	49.9K
4 Cell (4S1P)	4.5A	95.3K	49.9K
4 Cell (2S2P)	8A	32.4K	49.9K

Battery	UVP	R5	R6
6 Cell (3S2P)	9V	78.7K	49.9K
4 Cell (4S1P)	12V	46.4K	49.9K
4 Cell (2S2P)	6V	143K	49.9K


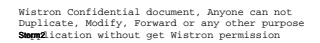
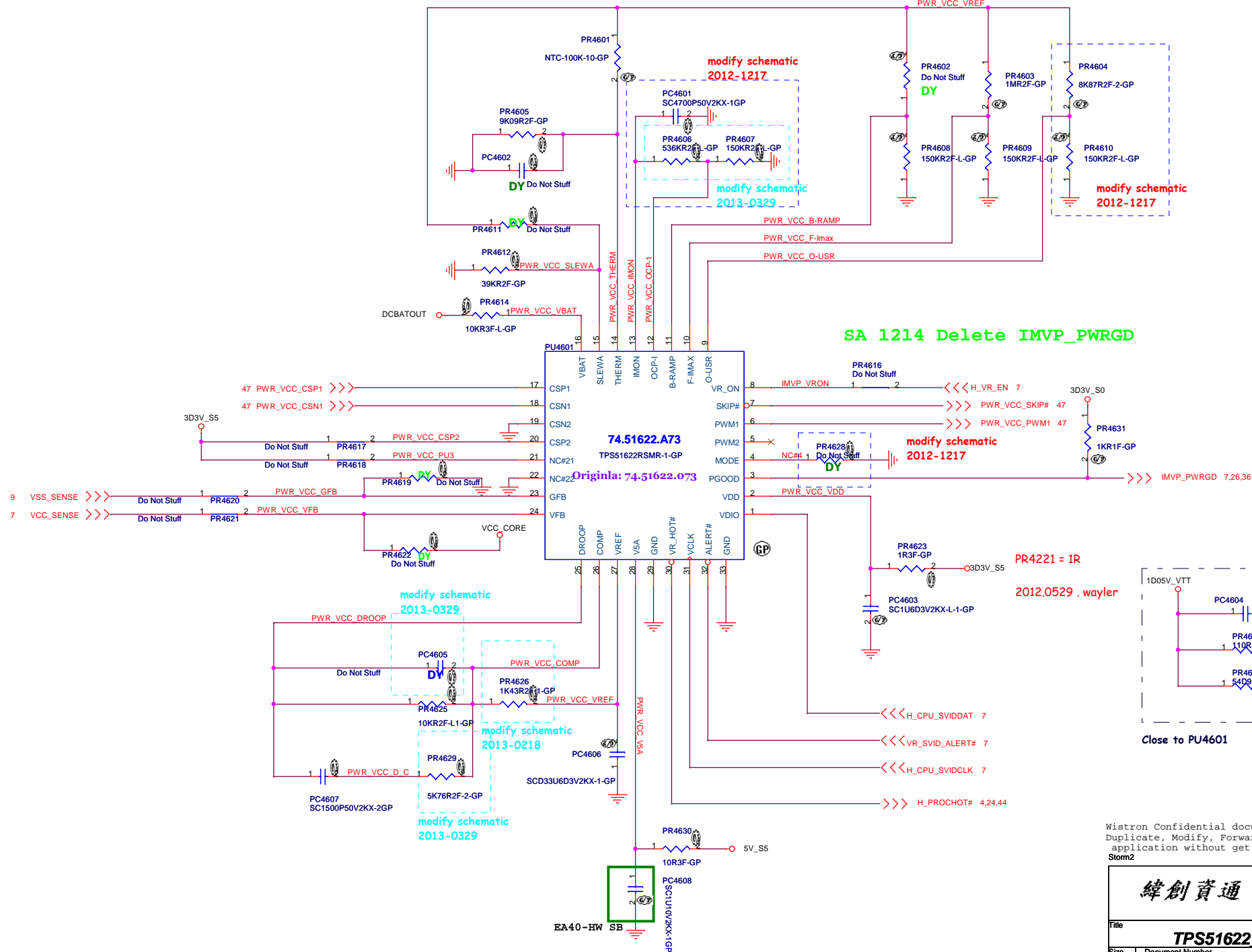
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緯創資通			
Title			
CHARGER BQ24737			
Size	Document Number		Rev
A4	Storm 2		-1
Date	Tuesday, April 02, 2013		102

Figure 10 shows two PCB layout sections. The left section is labeled '3D3V_PWR_DCBATOUT' and the right section is labeled '5V_PWR_DCBATOUT'. Both sections show a series of components connected in a chain. The components are labeled PG4501, PG4502, PG4503, and PT4502. The layout includes 'Do Not Stuff' labels for the components. The components are connected in a chain, with the output of one component connected to the input of the next. The layout also shows the connection to the 3D3V_PWR and 5V_PWR rails.



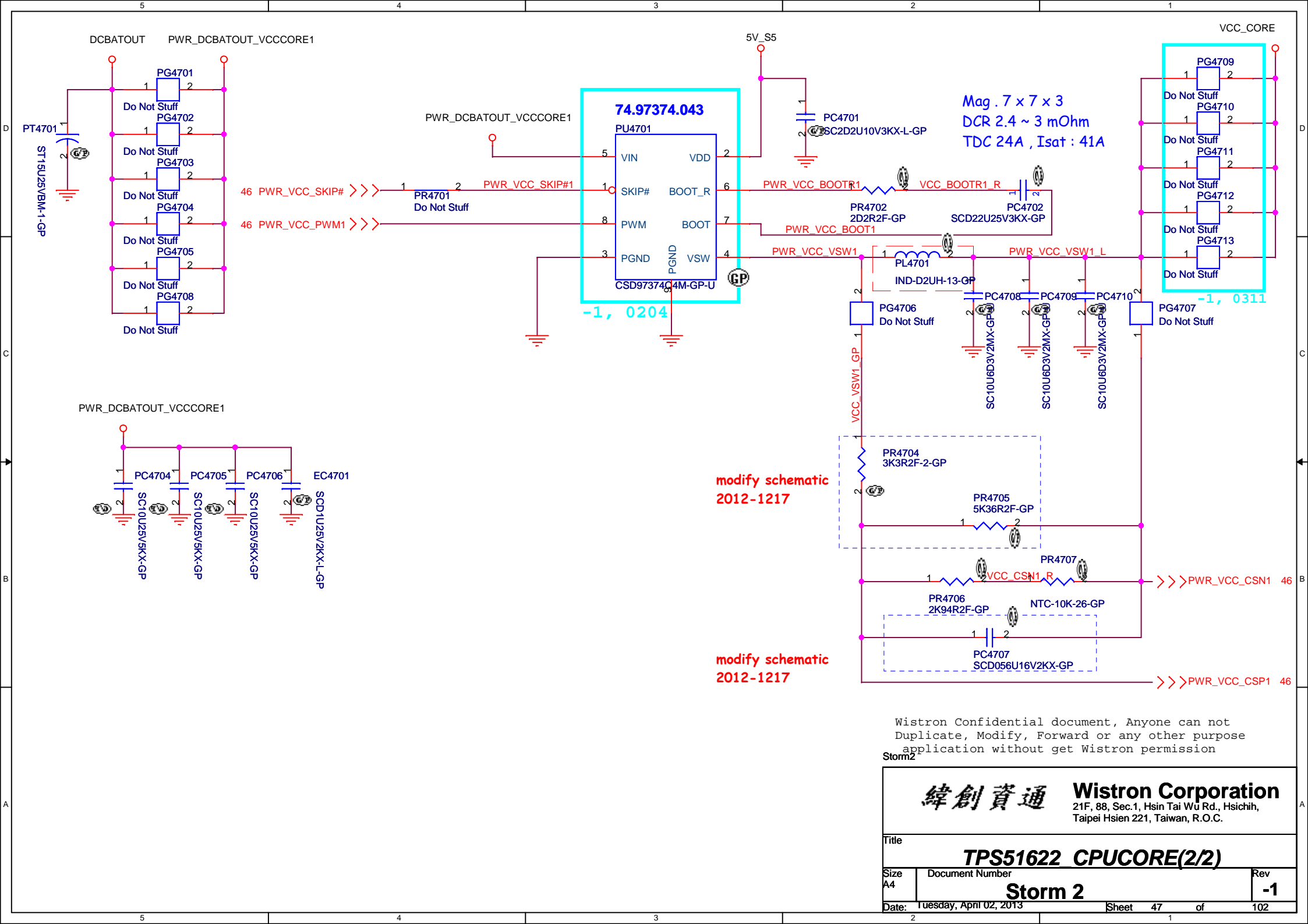
SSID = CPU_Regulator



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Title			TPS51622 CPUCORE(1/2)
Size	Document Number	Rev	-1
A3	Storm 2		
Date:	Monday, April 08, 2013	Sheet	46 of 102



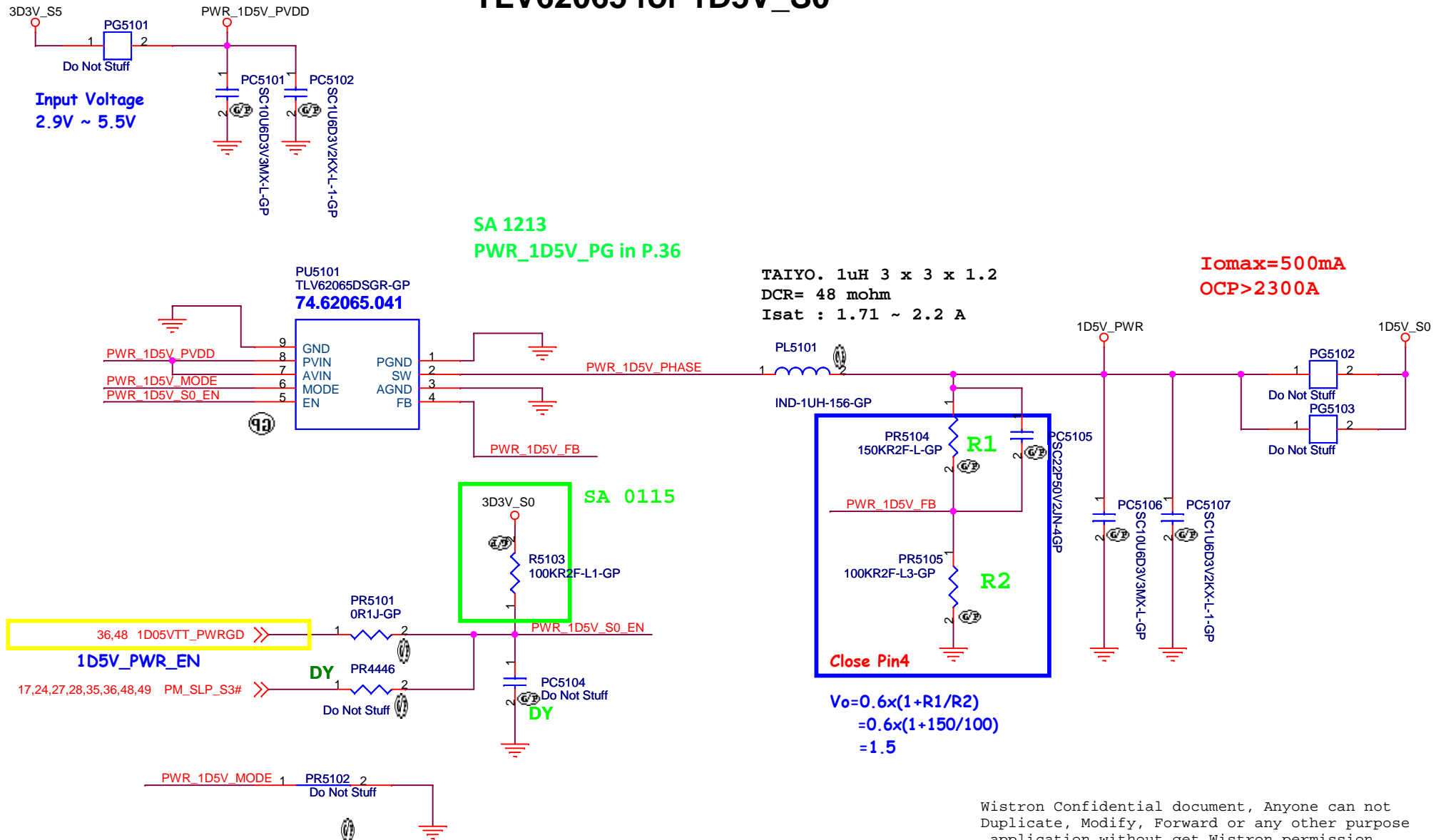
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Title 1D8V S0 (Reserved)		
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Date: Friday, December 28, 2012		Sheet 50 of 102

TLV62065 for 1D5V_S0



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MODE pin	Function
High	Fixed Freq. PWM mode
Low	Power Save Mode with automatic transition from PFM mode to fixed freq. PWM mode

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Title

1D5V S0 TLV62065

Size
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Document Number

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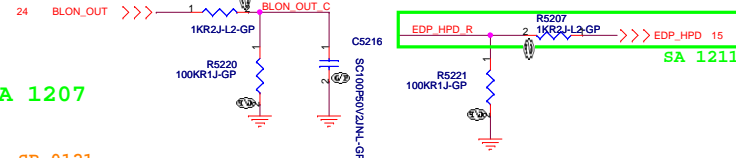
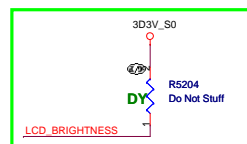
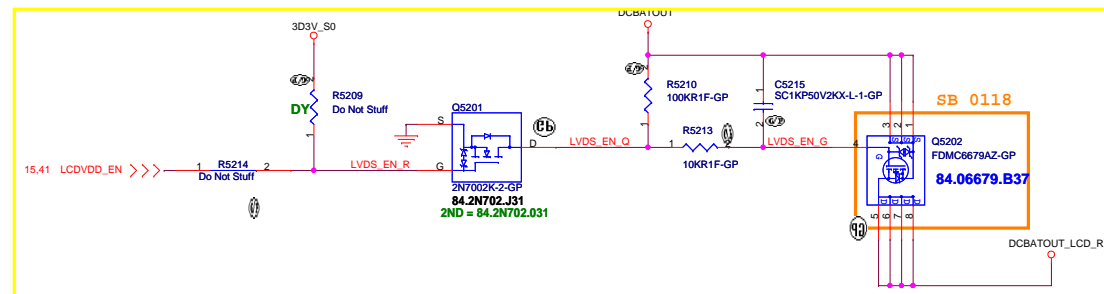
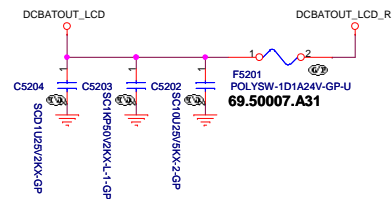
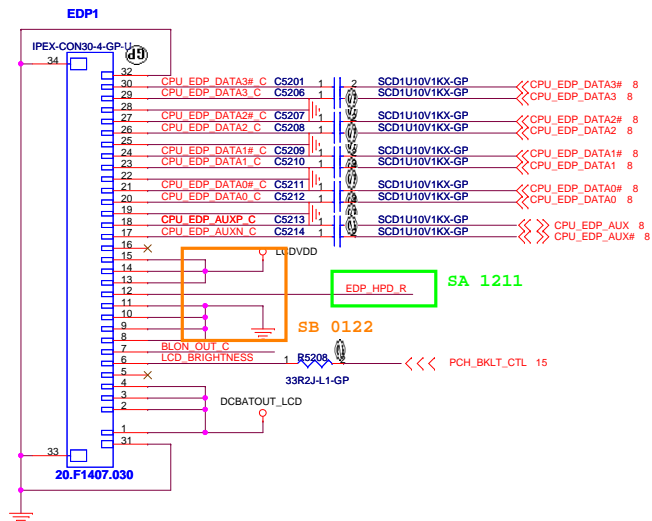
Rev
-1

Date: Tuesday, April 02, 2013

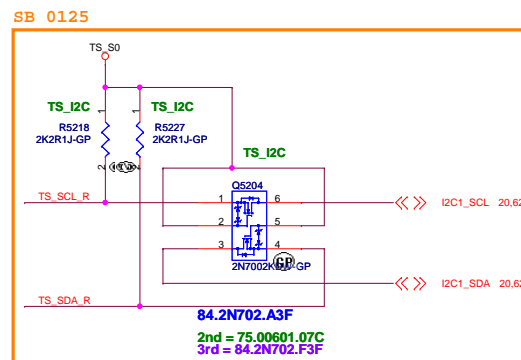
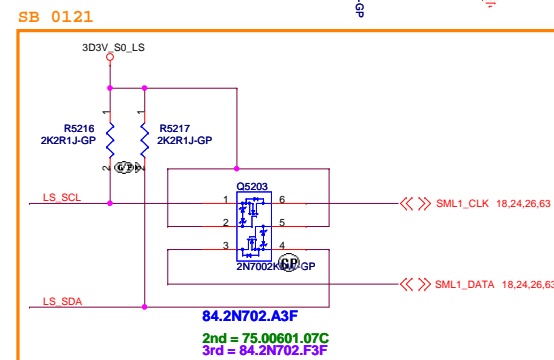
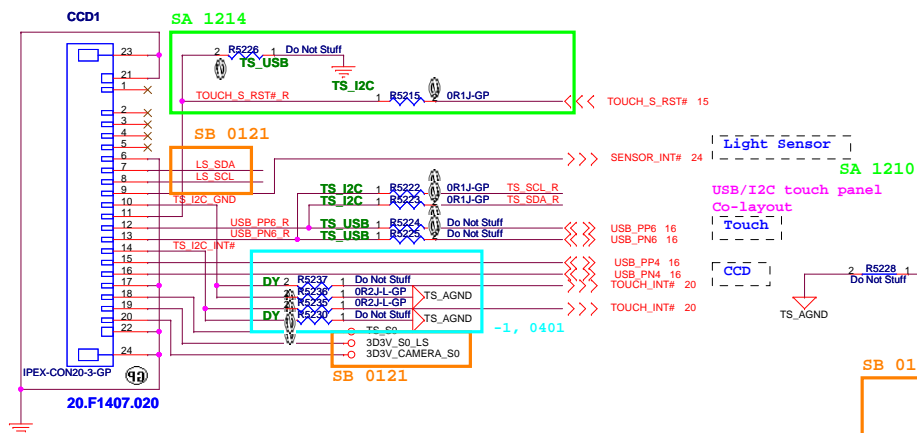
Sheet 51 of 102

EDP CONNECTOR

```
output turn-On Rising Time:1.3ms~2.7ms
current limit:2~3.3A
Previous parts(74.05285.07F)rise time:1.5ms ~5ms
current limit:1.5ms~ 3.5ms
```



CCD/TS/LS CONNECTOR



Storm / Helium / MA50 /
Petra / MA40 / Husk /MA52

Storm2 / Helium2 / Angel

USB / I2C interface pin define

USB interface pin define

Pin Assignment	
1	VBus
2	USB_dm
3	USB_DP
4	GND
5	GND
6	INT

Need to modify cable



USB		I2C(compatible)	
pin	define	pin	Define
1	VUSB_5V	1	+3.3V touch panel
2	USB_DM	2	SCL
3	USB_DP	3	SDA
4	UA_PA4	4	INT
5	GND	5	RESET
6	GND	6	GND

Need to rework component
to switch USB and I2C I/F on PCBs

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[illegible]**LCD/Inverter CONN**

Storm 2

Date: Wednesday, April 03, 2013

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5

4

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D

C

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B

B

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A

A

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Title			Reserved		
Size A4	Document Number Storm 2				Rev -1
Date: Friday, December 28, 2012			Sheet	53	of 102

5

4

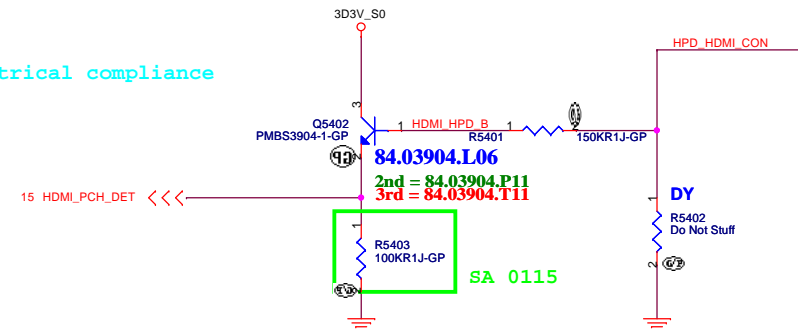
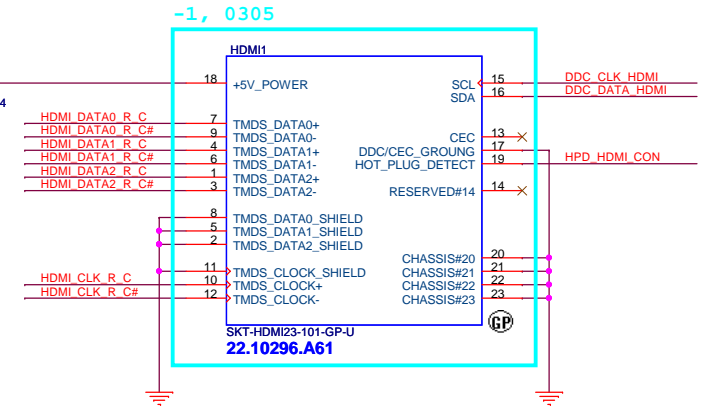
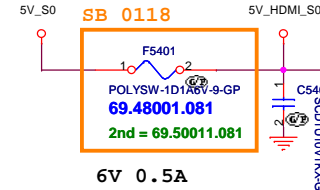
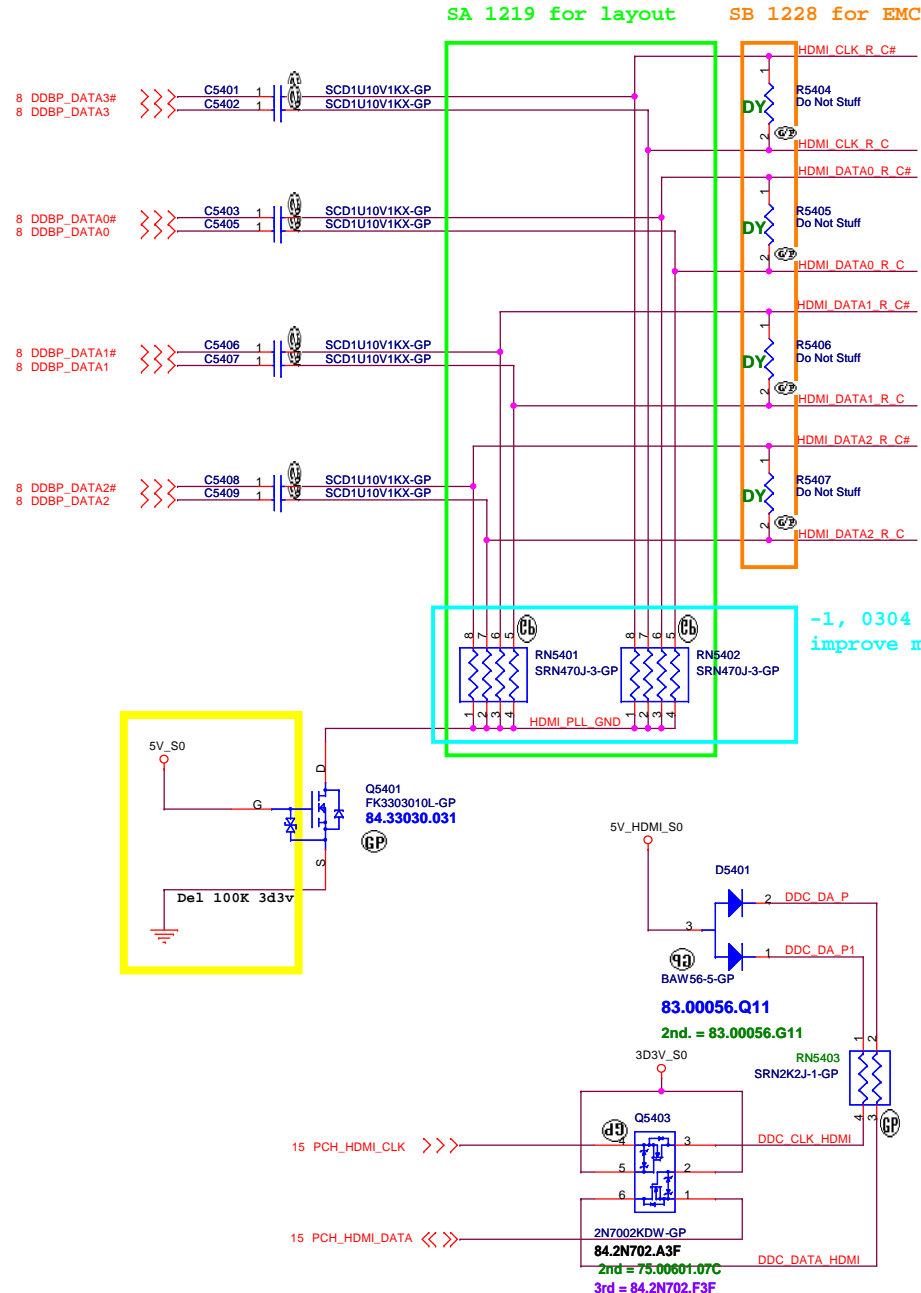
3

2

1

SSID = VIDEO

HDMI CONN.



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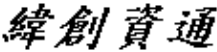
緯創資通 Wistron Corporation
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Title		
HDMI Level Shifter/Connector		
Size	Document Number	Rev
A3	Storm 2	-1
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Title NGFF_SSD (Reserved)		
Size A4	Document Number Storm 2	Rev -1
Date: Friday, December 28, 2012		Sheet 56 of 102

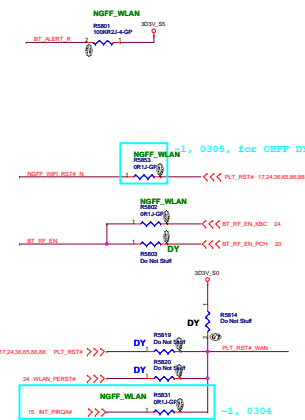
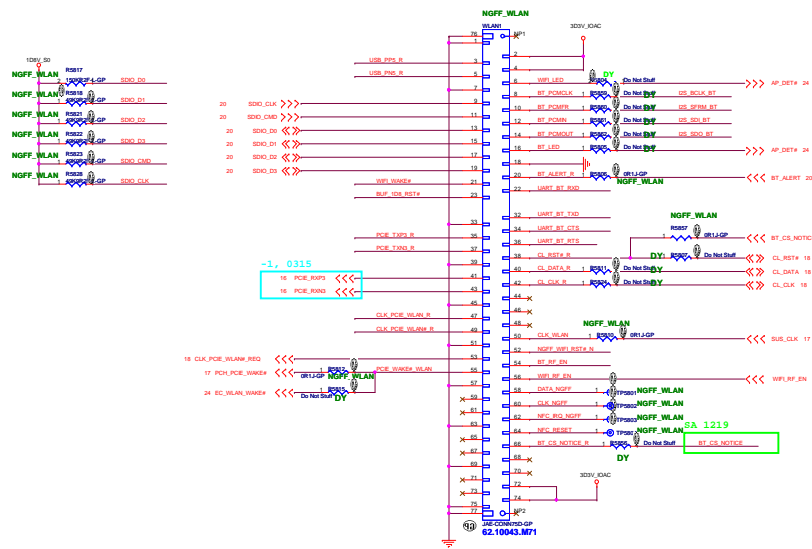
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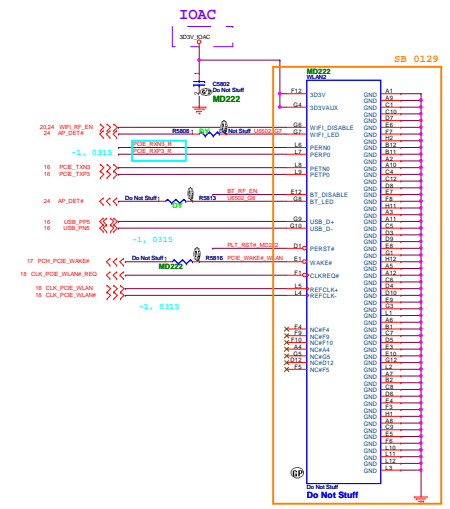
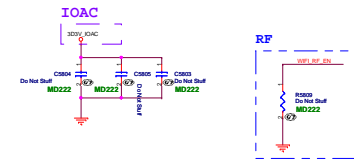
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Title			
Reserved			
Size	Document Number		Rev
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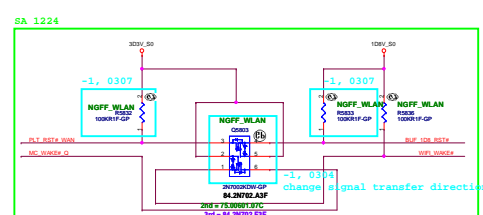
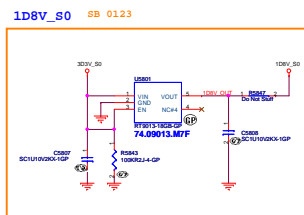
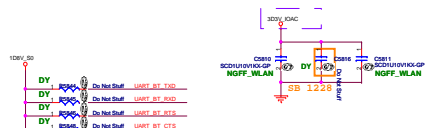
SSID = Wireless



```
SSID = Wireless
```



always low during S3 and S4 state with iRST

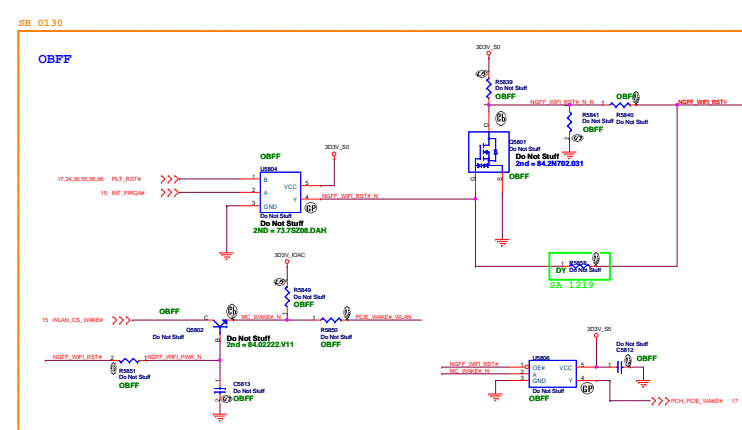
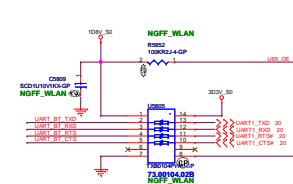
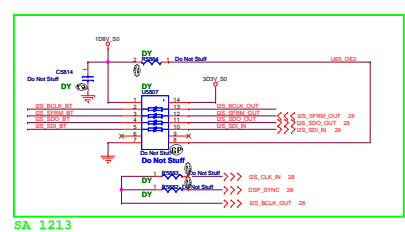


Co-layout with MD222 & NGFF

1. **1231 - change**

Place RS526 closed to WLAN1

Place RS529, RS530, RS534, RS535, RS542, RS555 closed to WLAN2



SSID = Wireless

NGFF Conn(WWAN) Reserved

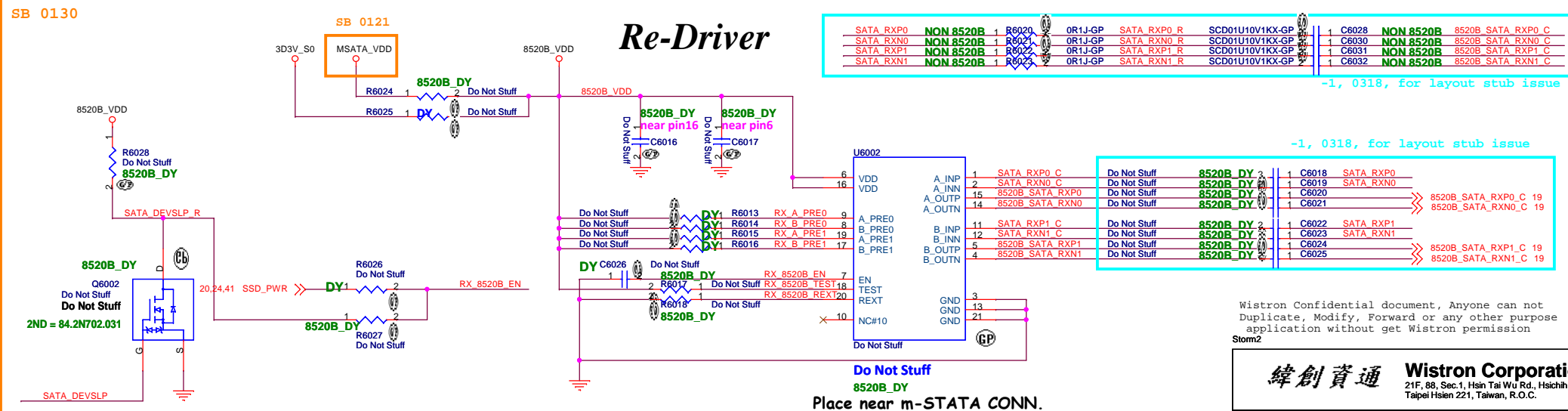
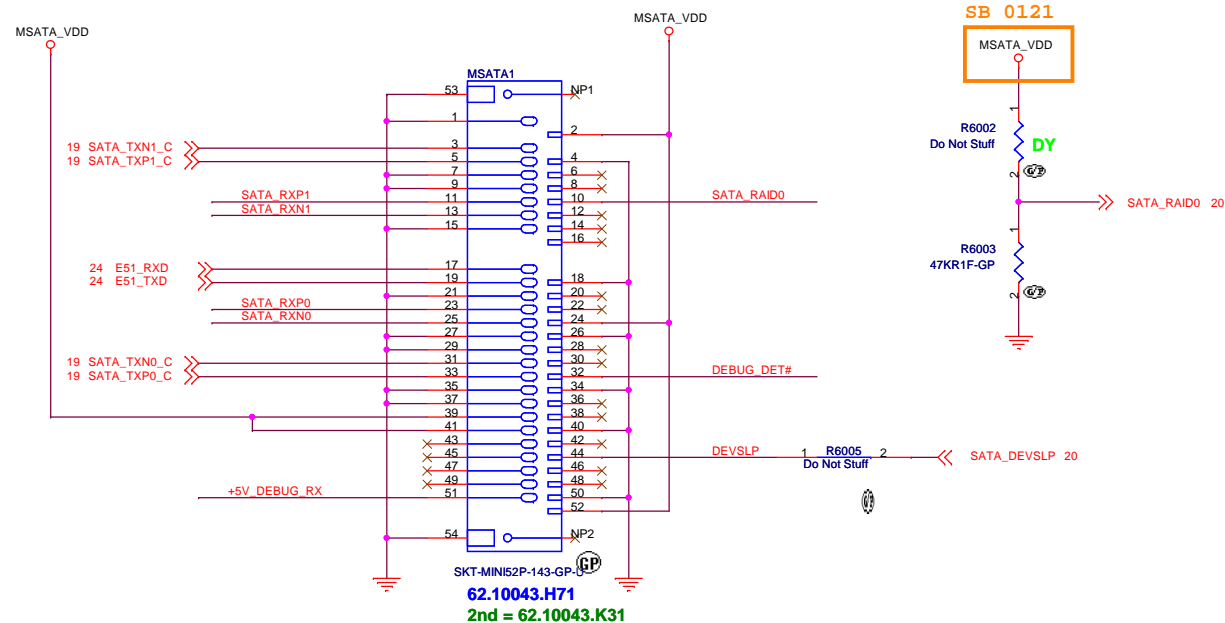
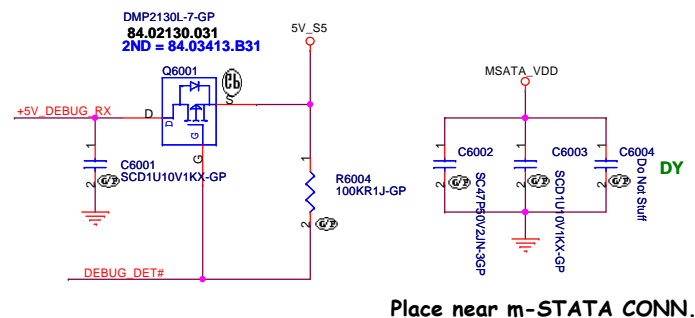
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Title reserved			
Size A4	Document Number Storm 2		Rev -1
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Mini Card Connector(mSATA)

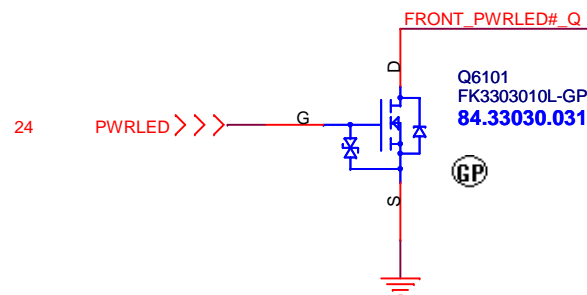


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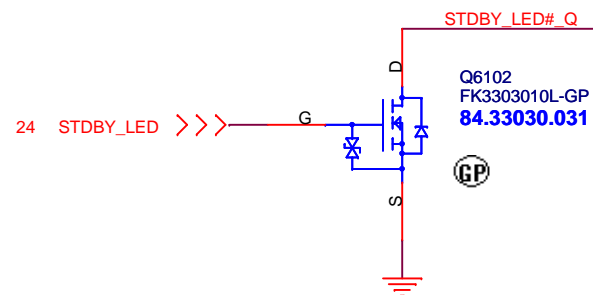
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

SSID = User.Interface

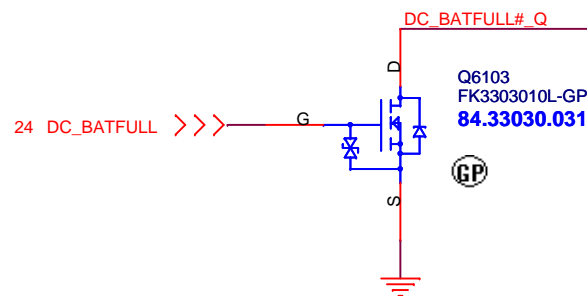
Power button LED



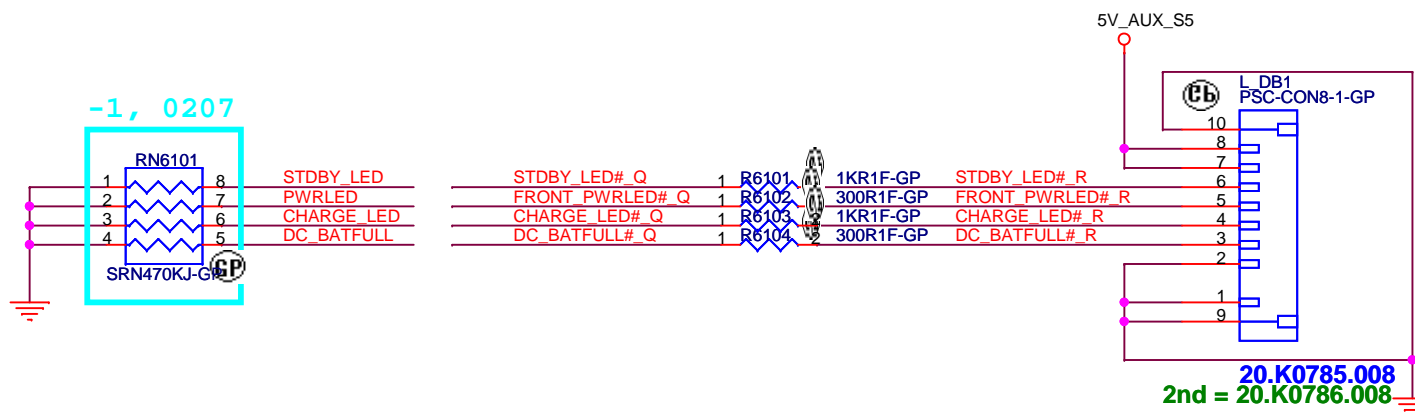
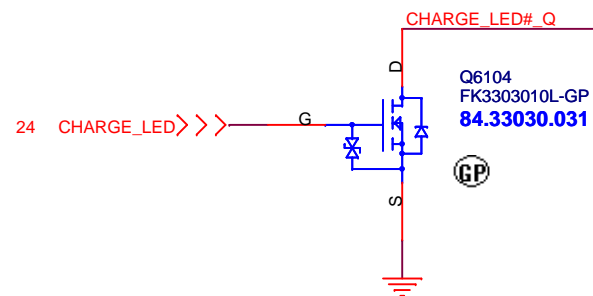
Power STDBY_LED



Battery LED2(DC_BATFULL)



Battery LED1(CHARGE)



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Title LED Board/Power Button

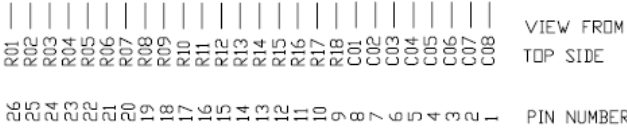
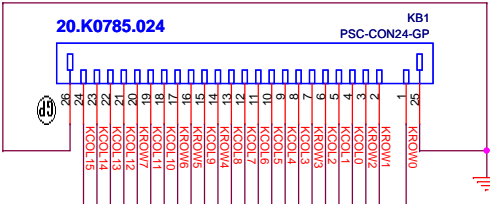
Size A4 Document Number Storm 2 Rev -1

Date: Tuesday, April 02, 2013 Sheet 61 of 102

Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VCC	VCC	VCC, 3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	NC		Not connected
3	NC		Not connected
4	GND	GND	Ground
5	I ² C_SDA	I/O	I ² C data. I _{Drive} or I _{Sink} : 8 mA max.
6	I ² C_SCL	I/O	I ² C clock I _{Drive} or I _{Sink} : 8 mA max.
7	/INT	O	Reserved for SMBUS application. Indicates touchpad likes to send data to system (host). Low active.
8	/Button		Low active, pulled to VCC through a 200K Ω resistor inside touchpad when touchpad is powered. Suggest pulled to VCC through a suitable resistor in system side when touchpad is powered off. Low when button is pressed.

Internal KeyBoard Connector

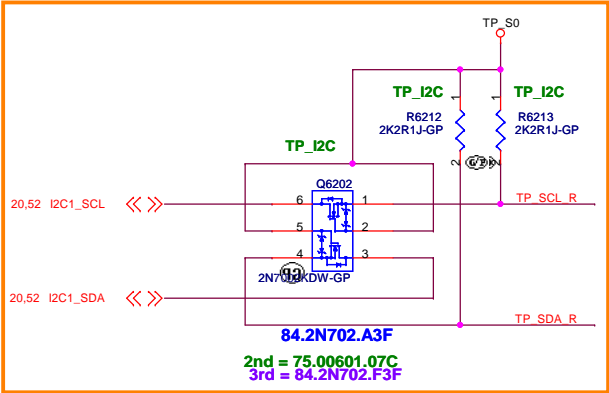
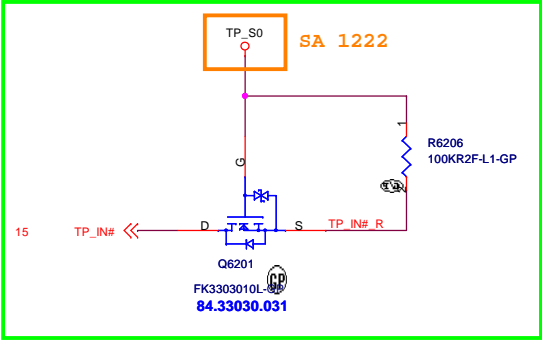
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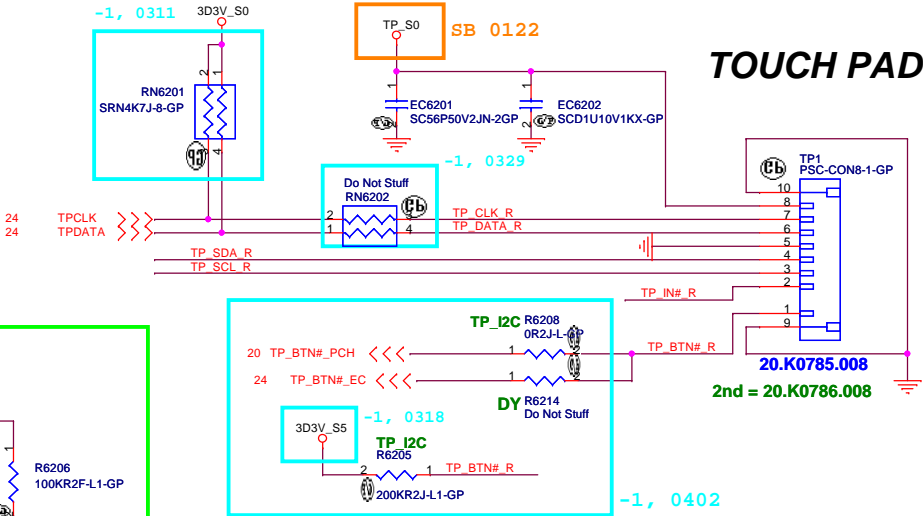
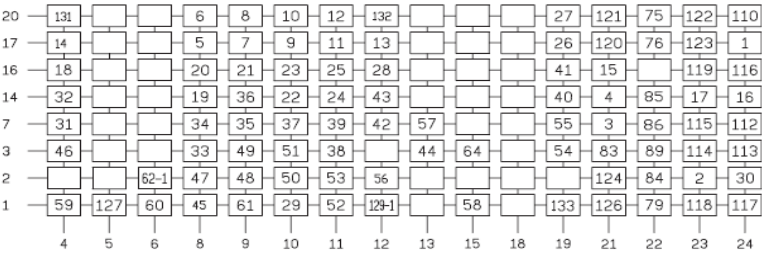
Pin number	Pin Define
1	VDD(3.3V)
2	PCClk
3	PCDt
4	DGND
5	NC*(S<DA>)
6	NC*(S<CL>)
7	NC*(S<INT>)
8	NC

Note: Reserve for SMBus

SA 1218



0.5 pitch



I2C Addr. = 0X20H (Synaptics)

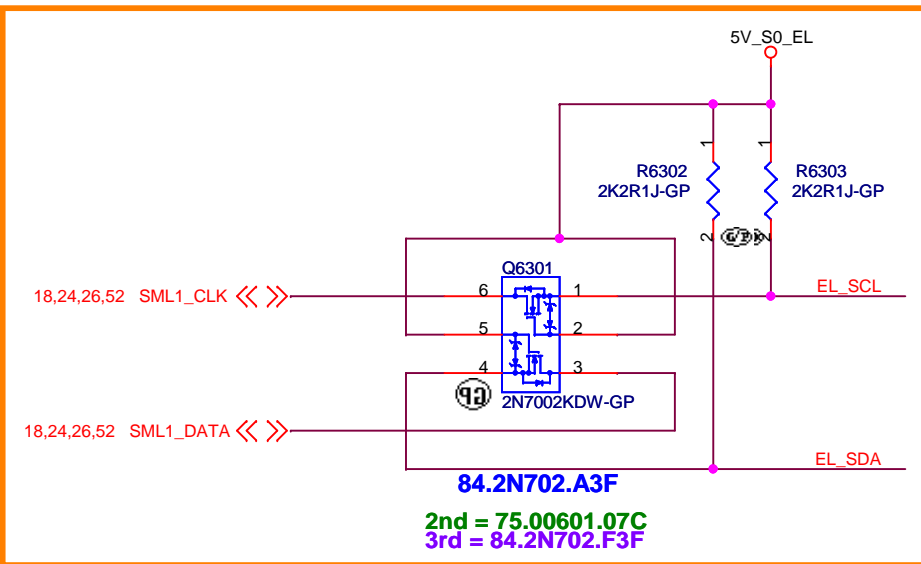
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Wistron Corporation
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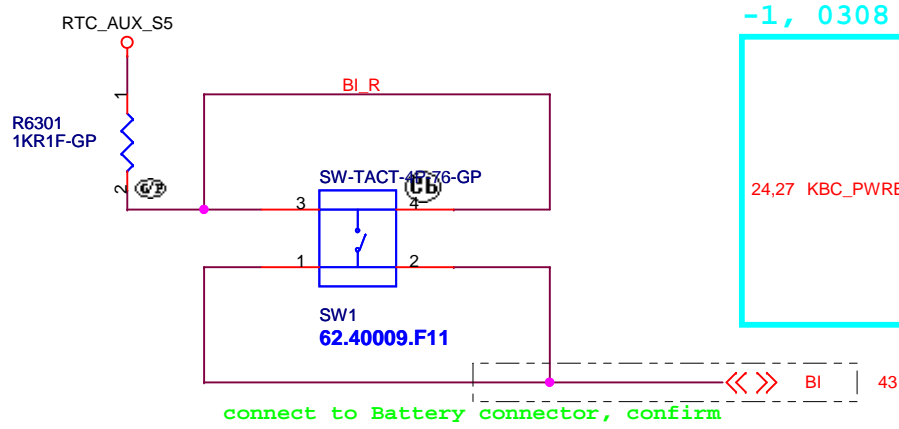
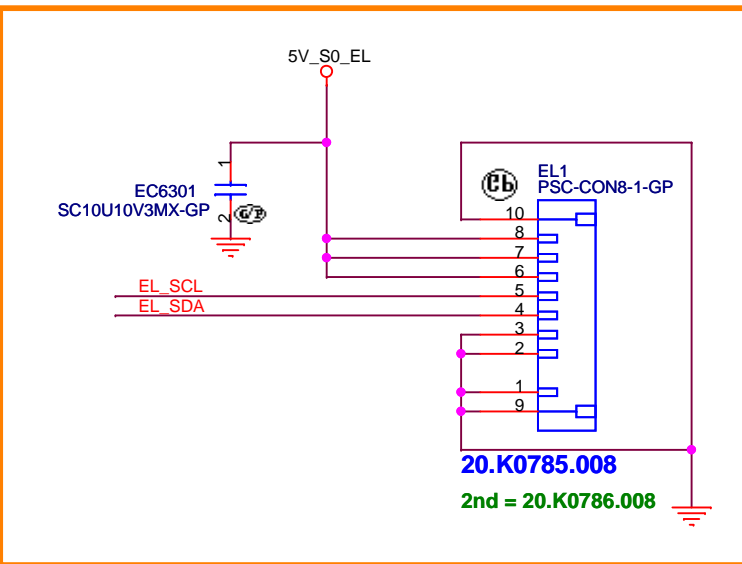
Key Board/Touch Pad		
Size A3	Document Number	Rev
	Storm 2	-1
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EL Backlight

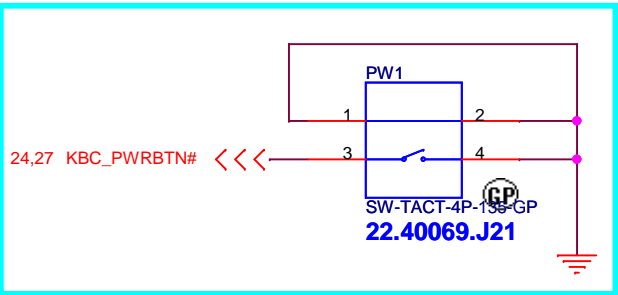
SB 0121



SB 1228



-1, 0308



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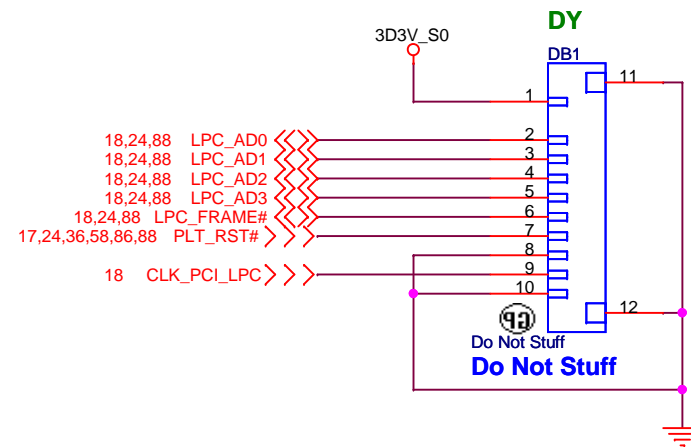
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Title			
IO Board Connector			
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Title <div>Hall Sensor (Reserved)</div>		
Size <div>A4</div>	Document Number <div>Storm 2</div>	Rev <div>-1</div>
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Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size
A4

Document Number

Storm 2

Rev
-1

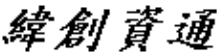
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Title <div>Thunderbolt 1/5 (Reserved)</div>		
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GPU VRAM I/F (Reserved)		
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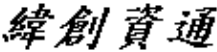
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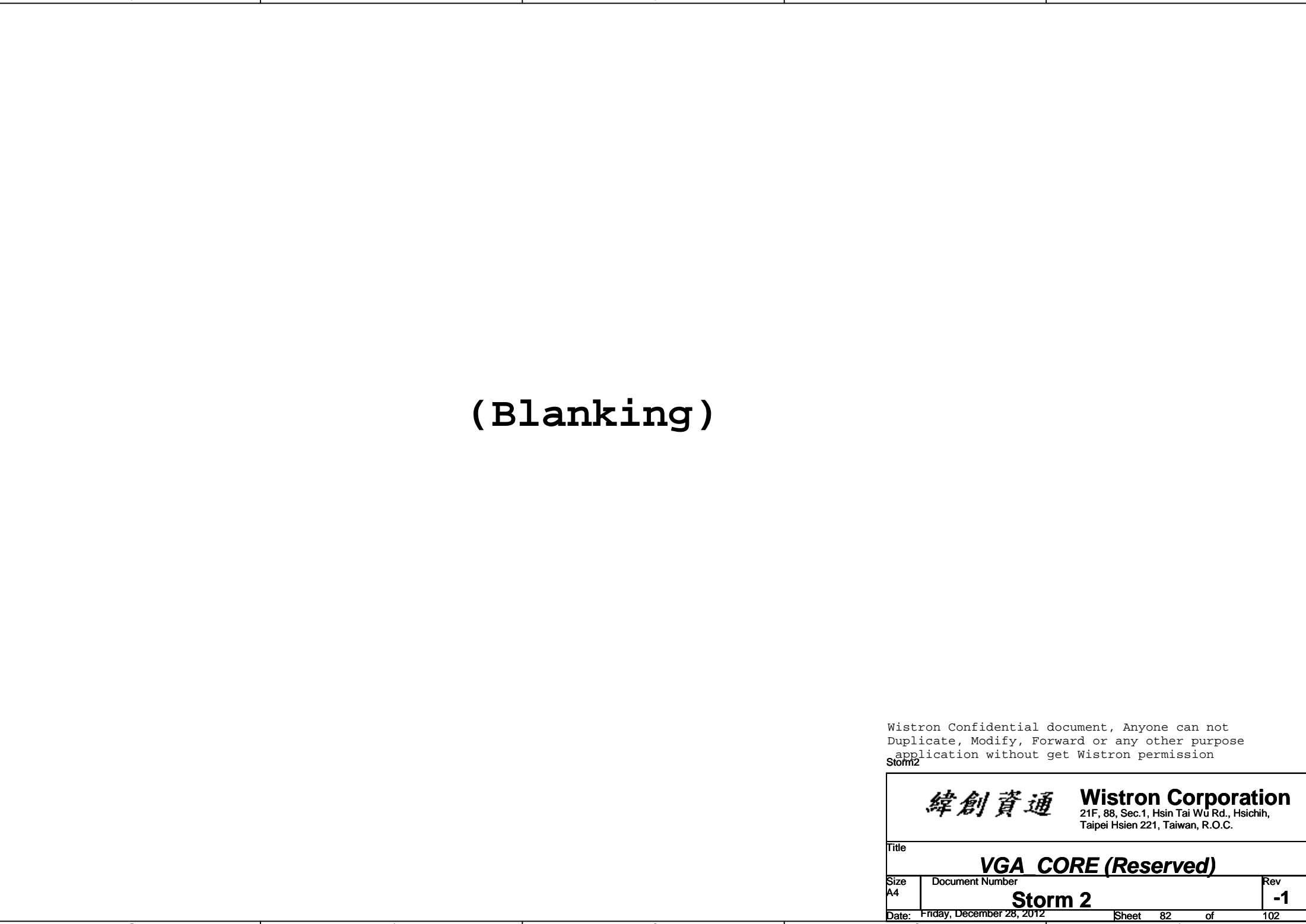
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Size	Document Number	Rev
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Title Switchable LCD (Reserved)		
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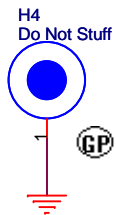
Do Not Stuff



Do Not Stuff



Do Not Stuff

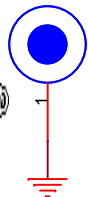


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SB 0118

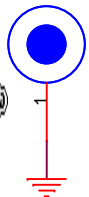
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HS1
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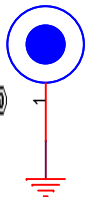
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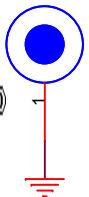
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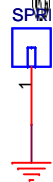
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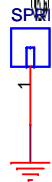
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SPRING-115-GP



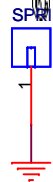
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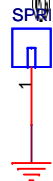
34.4PT16.001

S3
SPRING-115-GP



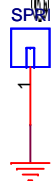
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S4
SPRING-115-GP



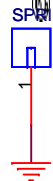
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S5
SPRING-115-GP



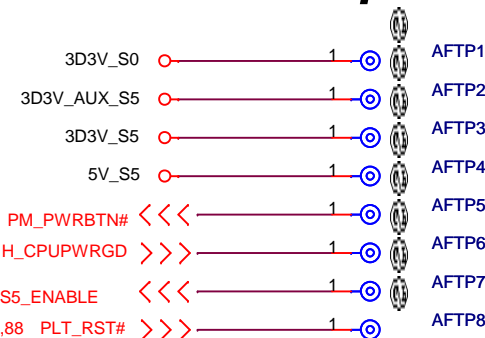
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S6
SPRING-115-GP



SB 0123

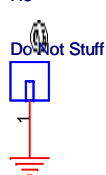
Check test point



Do Not Stuff

GNDPADS213X99-NP

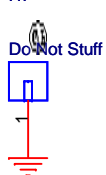
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Do Not Stuff

GNDPADS213X99-NP

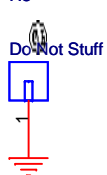
H7



Do Not Stuff

GNDPADS213X99-NP

H8



Do Not Stuff

GNDPADS213X99-NP

H9



Do Not Stuff

GNDPADS213X99-NP

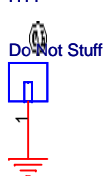
H10



Do Not Stuff

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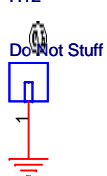
H11



Do Not Stuff

GNDPADS213X99-NP

H12



Do Not Stuff

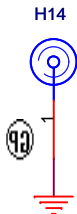
GNDPADS213X99-NP

H13



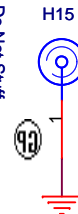
Do Not Stuff

H14



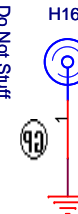
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H15



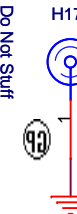
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H16



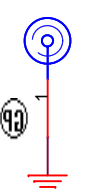
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H17



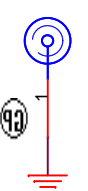
Do Not Stuff

H18



Do Not Stuff

H19



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Title

UNUSED PARTS/EMI Capacitors

Size

Document Number

Rev

Storm 2

-1

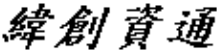
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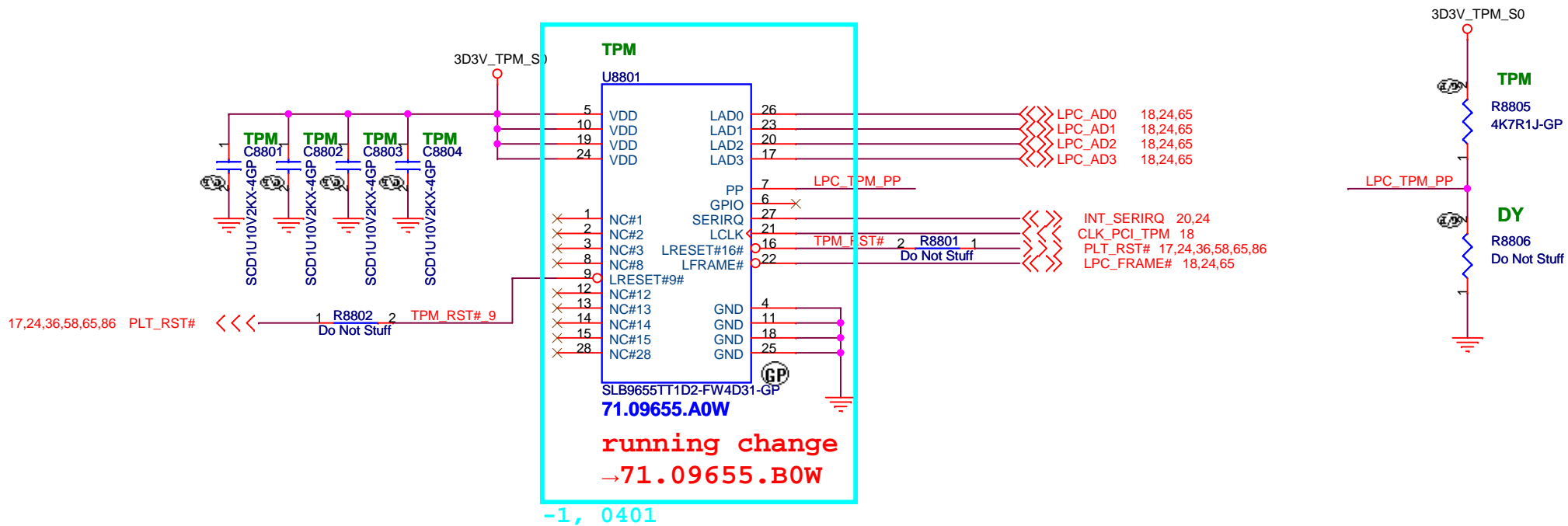
Sheet 86 of 102

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NFC Connector			
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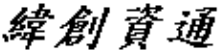
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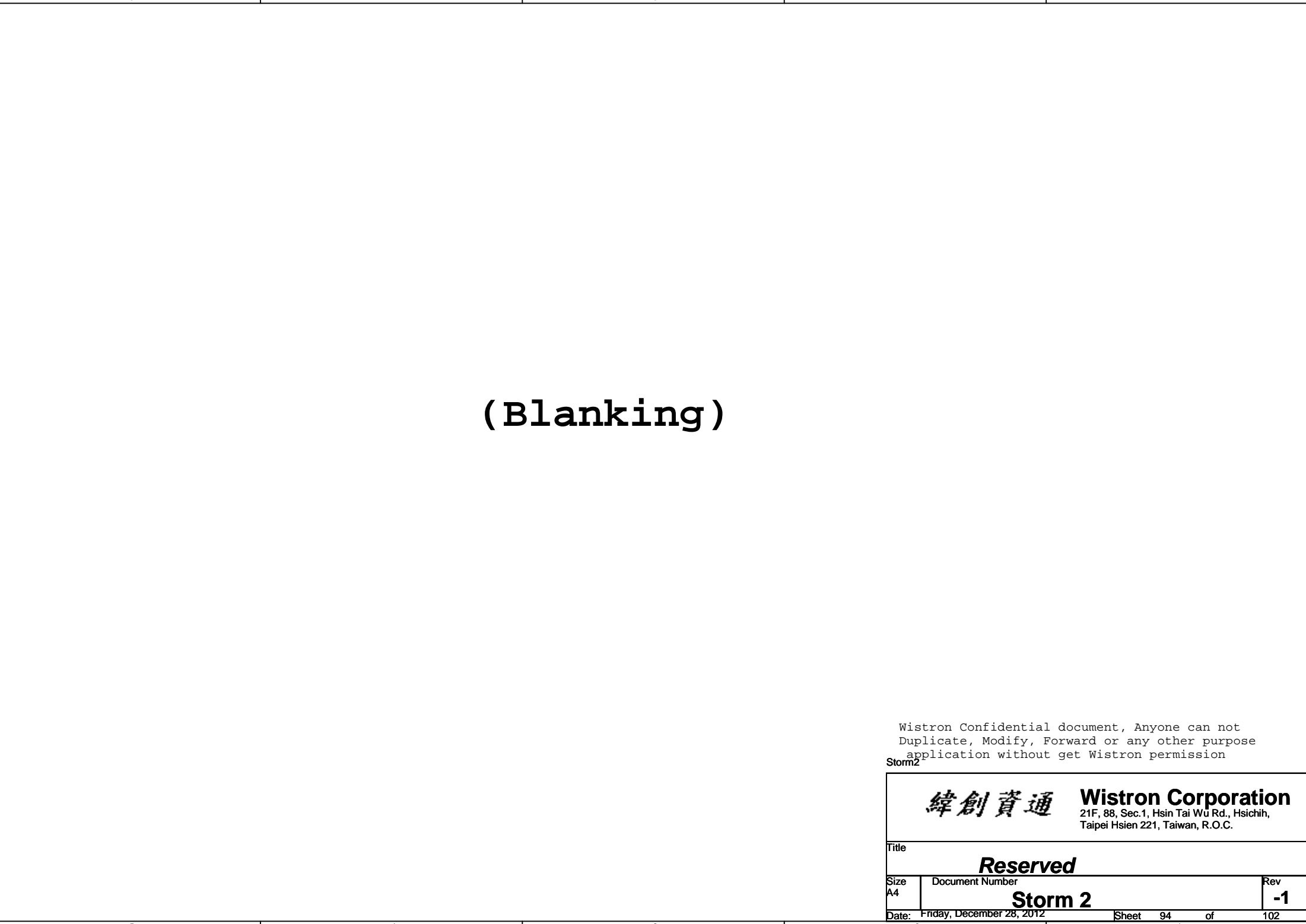
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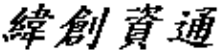
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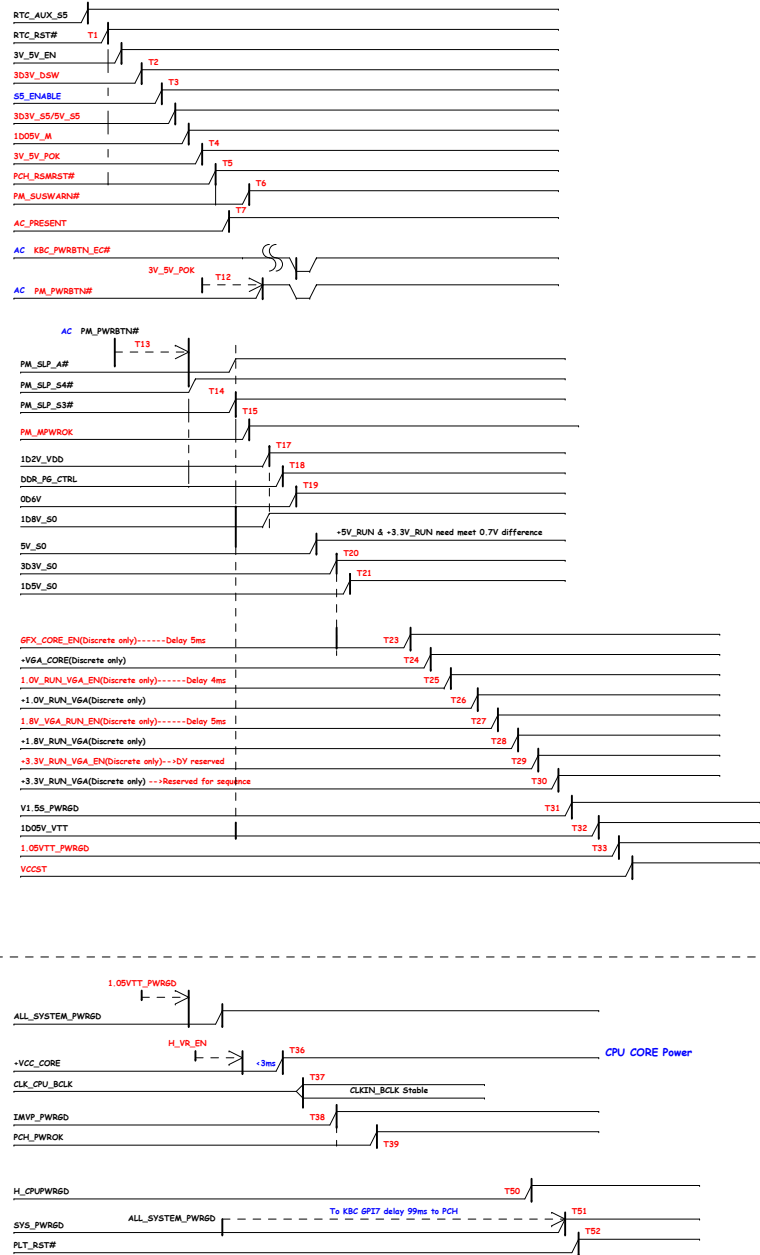
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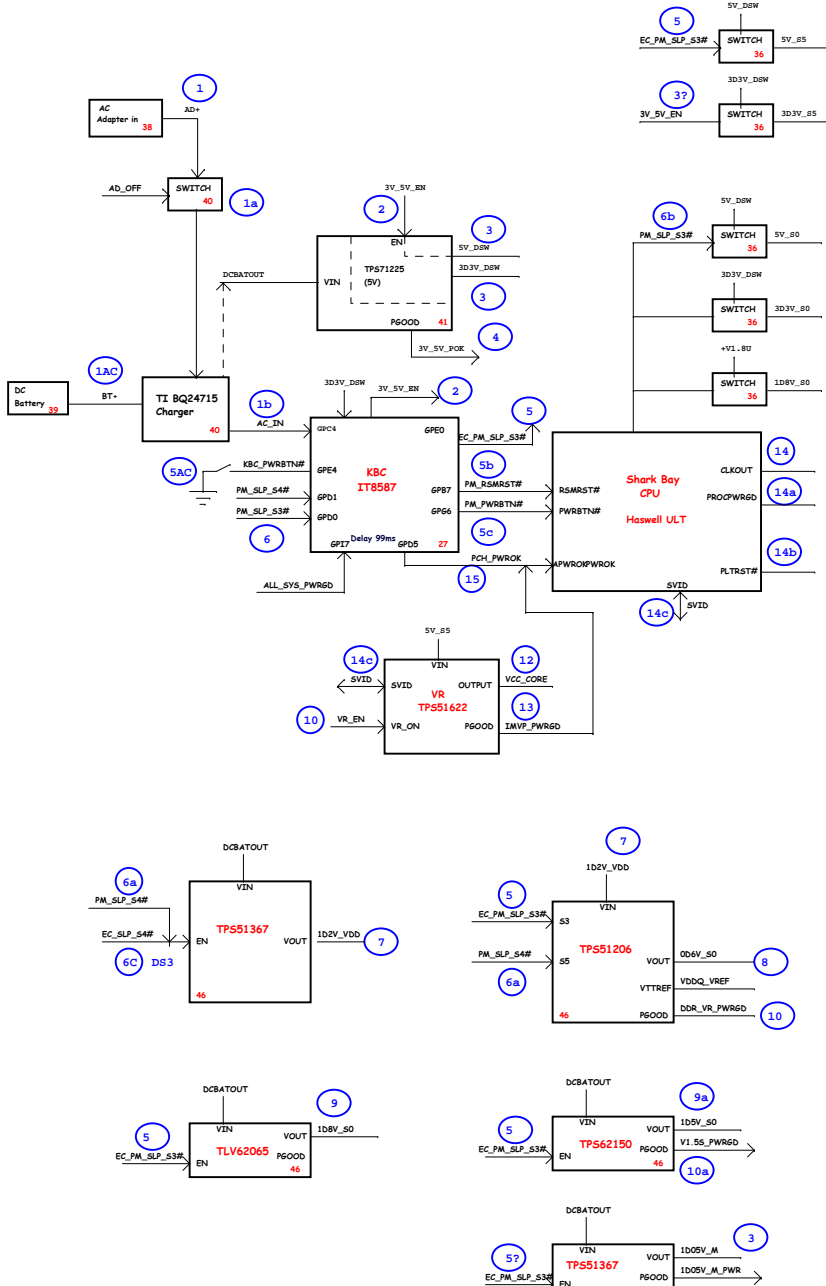
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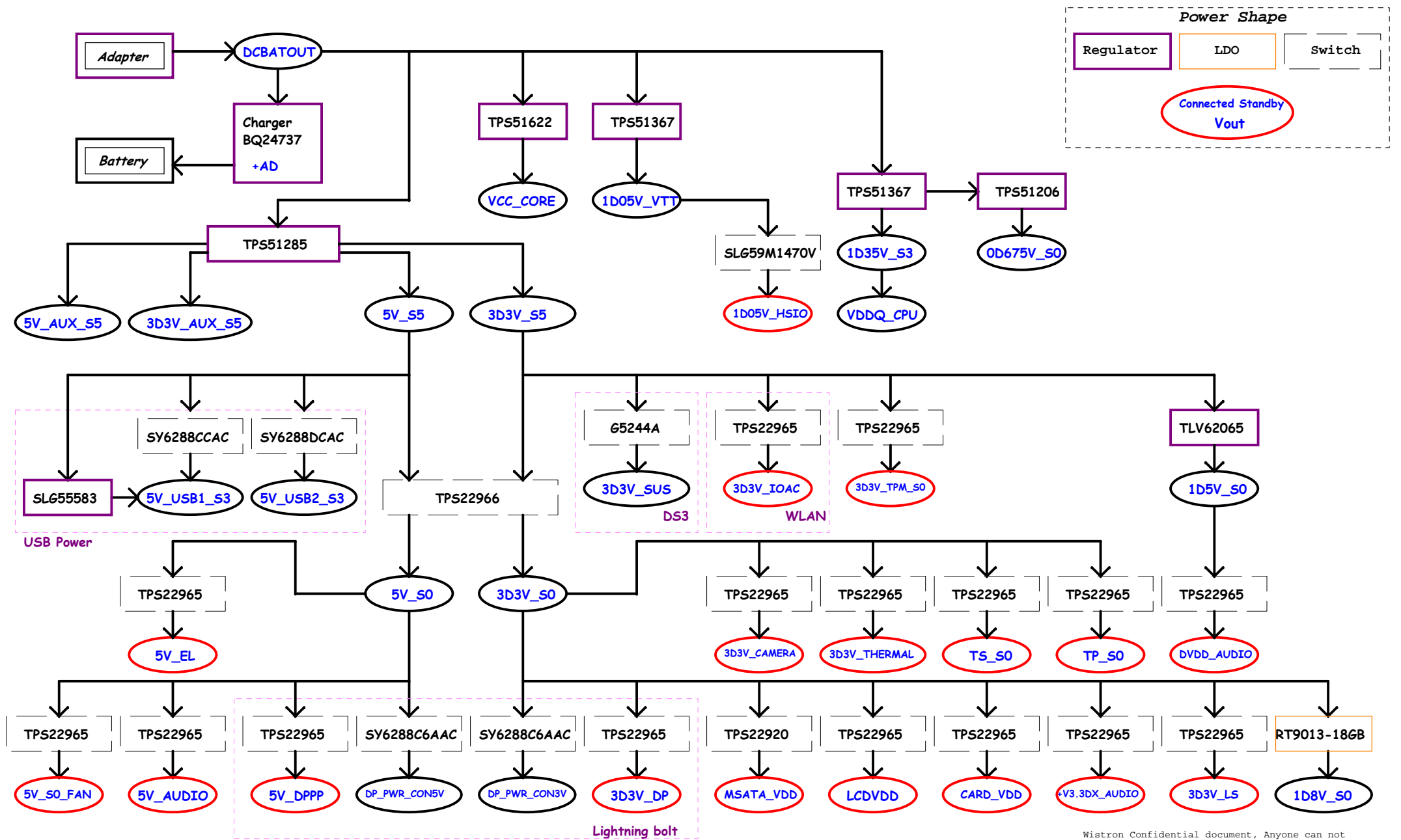
Intel-Power Up Sequence

(AC mode)



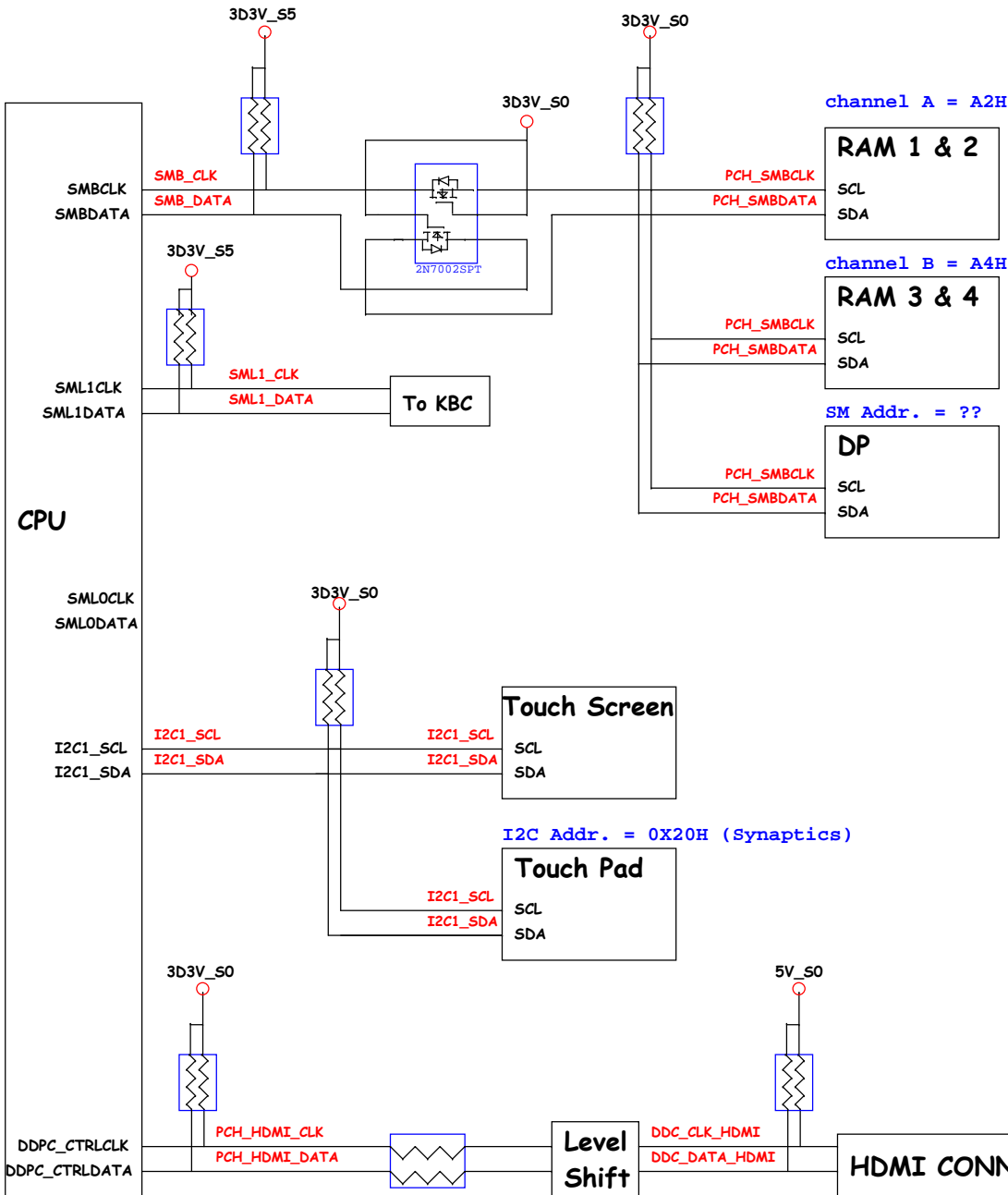
SHARK BAY POWER UP SEQUENCE DIAGRAM



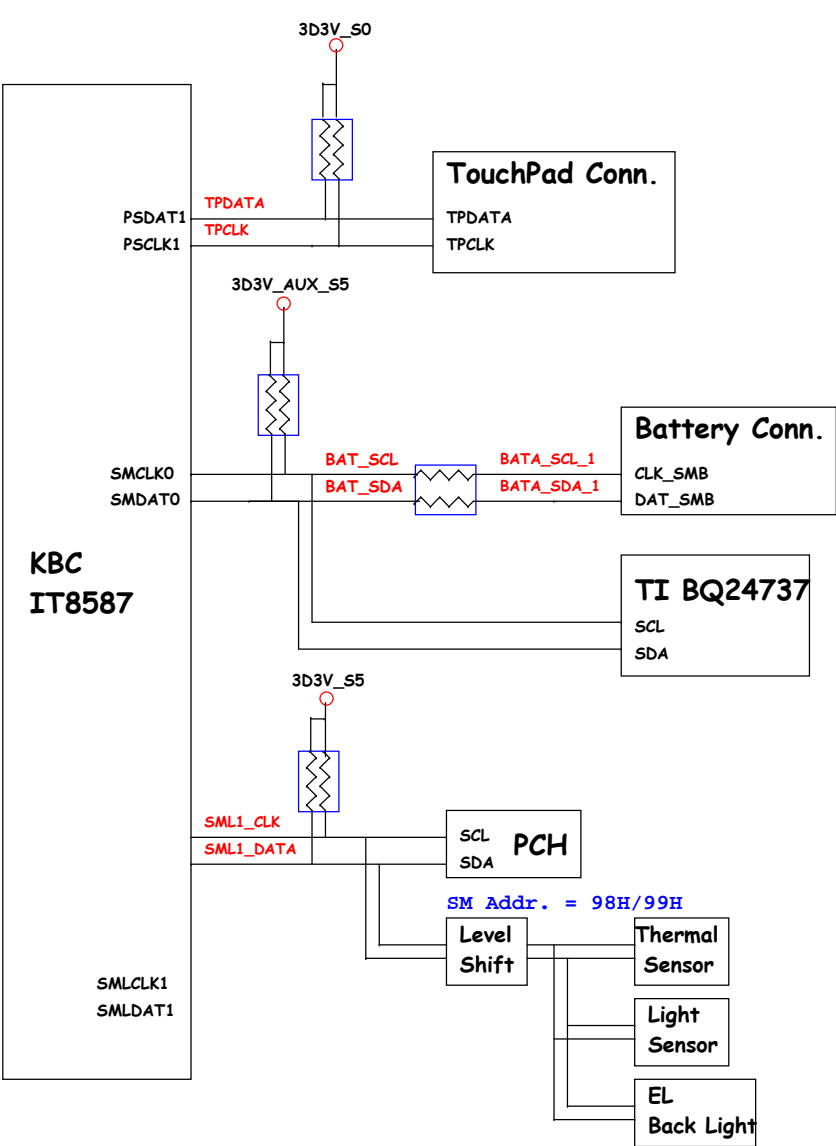


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CPU SMBus Block Diagram

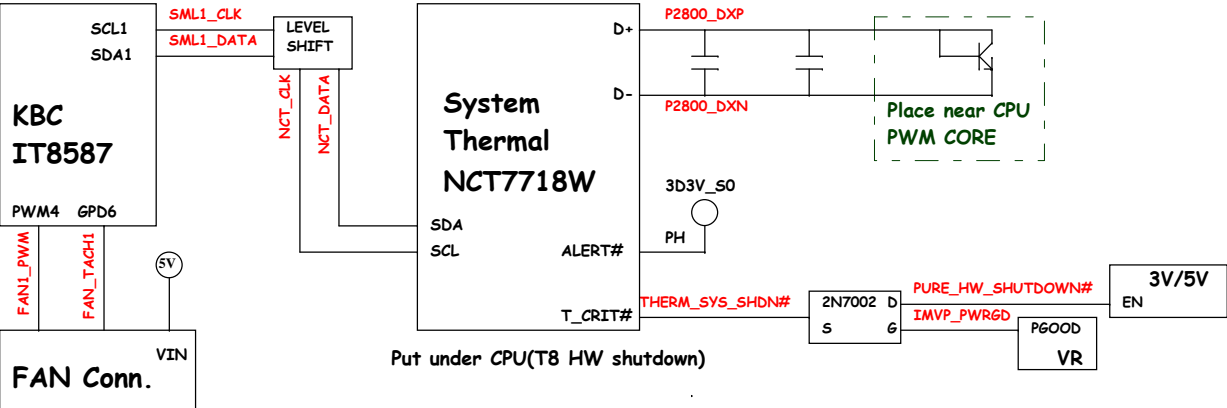


KBC SMBus Block Diagram

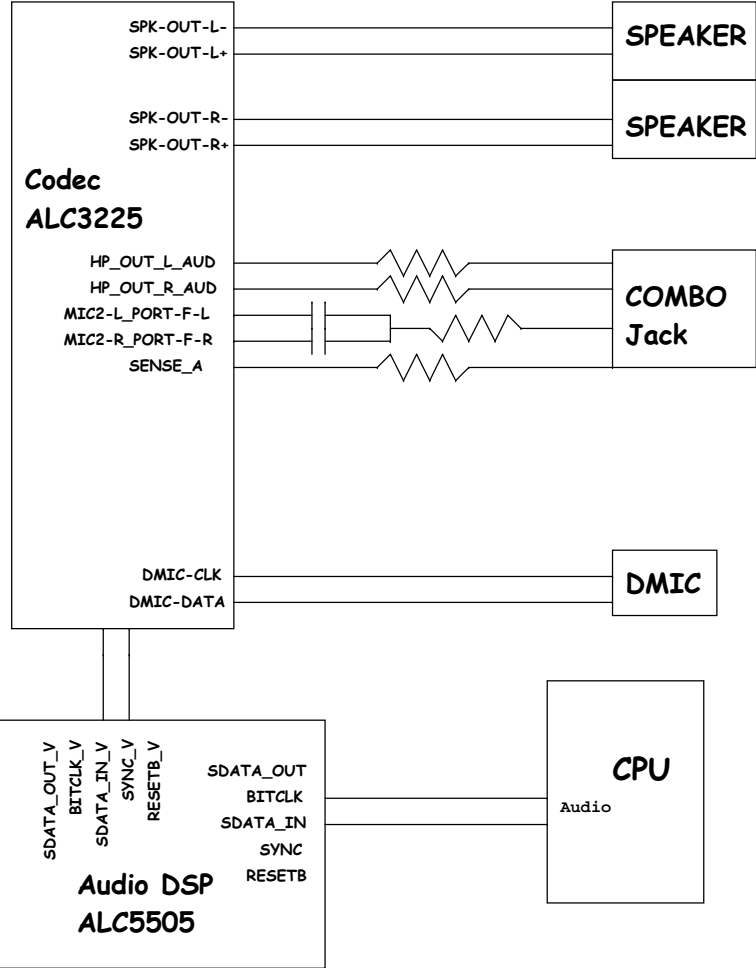


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Thermal Block Diagram



Audio Block Diagram



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