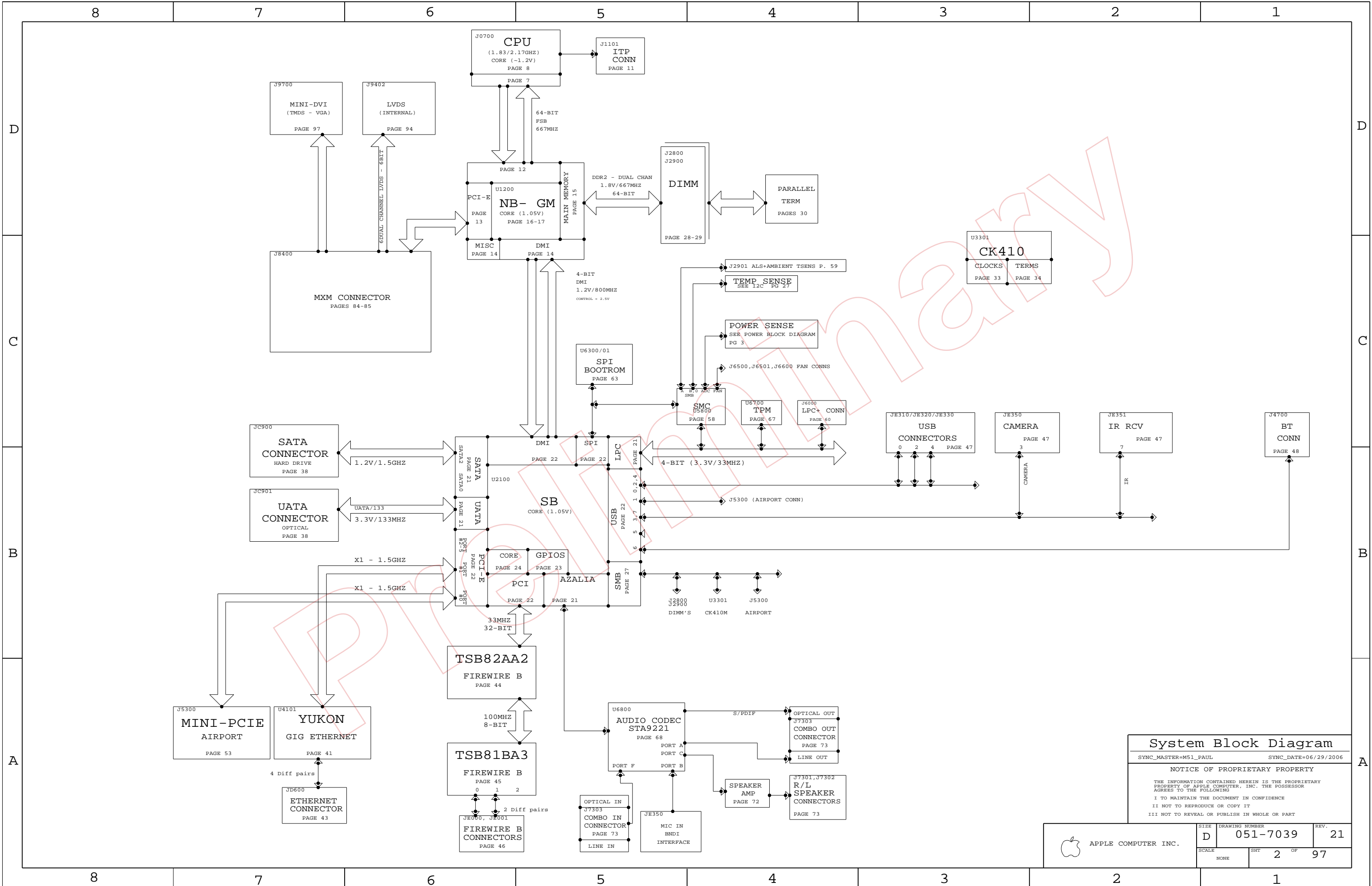


8		7		6		5		4		3		2		1			
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.												REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.												21		446951	ENGINEERING RELEASED	06/29/06	06/22/04
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.																	
SANTANA - M51 MLB																	
DVT -- 06/29/06																	
PDF CSA CONTENTS MASTER DATE												Schematic / PCB #'s					
2 2 System Block Diagram M51_PAUL 06/29/2006												PART# QTY DESCRIPTION REFERENCE DESIGNATOR(S) CRITICAL BOM OPTION					
3 3 Power Block Diagram M51_PAUL 06/29/2006												051-7039 1 PCB,SCHEM,MLB,M51 SCH1					
4 4 BOM Config M51_DAVE (MASTER)												820-1984 1 PCB,FAB,MLB,M51 MLB1					
5 5 FUNC TEST 1 OF 2 M51_HENRY 06/29/2006																	
6 6 POWER CONN / MISC M51_PAUL 06/29/2006																	
7 7 CPU 1 OF 2-FSB M50_HENRY 06/29/2006																	
8 8 CPU 2 OF 2-PWR/GND M50_HENRY 06/29/2006																	
9 9 CPU DECAPS & VID<> M51_HENRY 06/29/2006																	
10 10 ASIC TEMP SENSORS M51_DAVE (MASTER)																	
11 11 CPU ITP700FLEX DEBUG M50_HENRY 06/29/2006																	
12 12 NB CPU Interface M50_HENRY 06/29/2006																	
13 13 NB PEG / Video Interfaces M50_HENRY 06/29/2006																	
14 14 NB Misc Interfaces M50_HENRY 06/29/2006																	
15 15 NB DDR2 Interfaces M50_HENRY 06/29/2006																	
16 16 NB Power 1 M51_HENRY 06/29/2006																	
17 17 NB Power 2 M51_HENRY 06/29/2006																	
18 18 NB Grounds M50_HENRY 06/29/2006																	
19 19 NB (GM) Decoupling M51_DAVE (MASTER)																	
20 20 NB Config Straps M50_HENRY 06/29/2006																	
21 21 SB: 1 OF 4 M50_DOUG 06/29/2006																	
22 22 SB: 2 OF 4 M50_DOUG 06/29/2006																	
23 23 SB: 3 OF 4 M51_DOUG 06/29/2006																	
24 24 SB: 4 OF 4 M50_DOUG 06/29/2006																	
25 25 SB:DECOUPLING M51_DOUG 06/29/2006																	
26 26 SB: MISC M50_DOUG 06/29/2006																	
27 27 M51 SMBus Connections M51_DAVE (MASTER)																	
28 28 DDR2 SO-DIMM Connector AM51_HENRY 06/29/2006																	
29 29 DDR2 SO-DIMM Connector BM51_HENRY 06/29/2006																	
30 30 Memory Active Termination M50_HENRY 06/29/2006																	
31 31 Memory Vtt Supply M50_HENRY 06/29/2006																	
32 33 CLOCKS M50_HENRY 06/29/2006																	
33 34 CLOCKS: TERMINATIONS M51_HENRY 06/29/2006																	
34 38 Disk Connectors M51_DOUG 06/29/2006																	
35 41 ETHERNET CONTROLLER M50_DOUG 06/29/2006																	
36 42 ETHERNET MISC M51_DOUG 06/29/2006																	
37 43 ETHERNET CONNECTOR M51_DOUG 06/29/2006																	
38 44 FW: 1394B-LINK/PHY M51_DOUG 06/29/2006																	
39 45 FW: 1394B MISC M51_DOUG 06/29/2006																	
40 46 FIREWIRE CONNECTORS M51_DOUG 06/29/2006																	
41 47 USB Device Interfaces M51_DOUG 06/29/2006																	
42 53 AIRPORT CONN M51_DOUG 06/29/2006																	
43 54 PCI-E CONNECTIONS M51_DOUG 06/29/2006																	
44 58 SMC M51_HENRY 06/29/2006																	
45 59 SMC & TPM SUPPORT M51_HENRY 06/29/2006																	
46 60 LPC+ CONN M51_HENRY 06/29/2006																	
47 63 SPI BOOTROM M50_DOUG 06/29/2006																	
48 65 HD AND OD FAN M51_HENRY 06/29/2006																	
49 66 CPU FAN, HD & OD TEMP M51_HENRY 06/29/2006																	
50 67 TPM M51_HENRY 06/29/2006																	
51 68 AUDIO: CODEC AUDIO 06/29/2006																	
52 69 AUDIO: LINE INPUT AMP AUDIO 06/29/2006																	
53 70 AUDIO: COMBO OUT AMP AUDIO 06/29/2006																	
54 71 AUDIO: SPEAKER AMP_1 AUDIO 06/29/2006																	
55 72 AUDIO: SPEAKER AMP AUDIO 06/29/2006																	
56 73 AUDIO: CONNECTORS AUDIO 06/29/2006																	
57 74 AUDIO: POWER SUPPLIES AUDIO 06/29/2006																	
58 75 IMVP6 CPU VCore Regulator M51_PAUL 06/29/2006																	
59 76 CPU & SYSTEM SENSE M51_DAVE (MASTER)																	
60 77 PWR GOOD M51_PAUL 06/29/2006																	
61 78 3V DC/DC 2.5V M51_PAUL 06/29/2006																	
62 79 1.8V & 1.2V VREG M51_PAUL 06/29/2006																	
63 80 1.5V_S0 & 1.05V_S0 VREG M51_PAUL 06/29/2006																	
64 82 5V DC/DC M50_PAUL 06/29/2006																	
65 83 S0 AND S3 FETS M51_PAUL 06/29/2006																	
66 84 MXM PCI-E & PWR M51_DAVE (MASTER)																	
67 85 MXM I/O M51_DAVE (MASTER)																	
68 94 Internal Display Conns M51_DAVE (MASTER)																	
69 97 External Display Conns M51_DAVE (MASTER)																	
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XX : _____												DRAWER		DESIGN CR			
X.XX : _____												ENG APPD		MFG APPD			
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THIRD ANGLE PROJECTION														DRAWING NUMBER 051-7039 REV. 21			
														SHT 1 OF 97			
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System Block Diagram

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

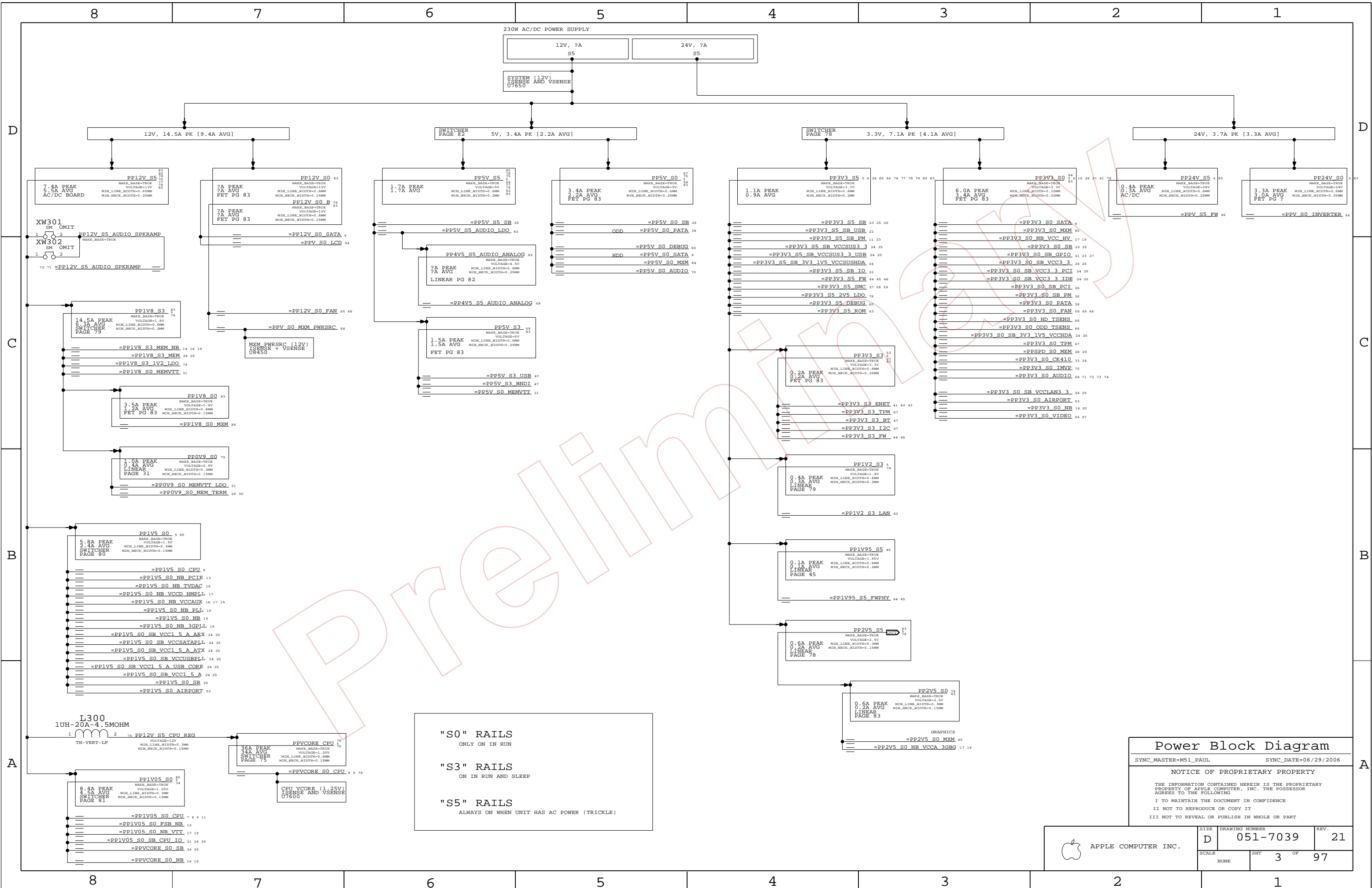
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	2	97



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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE	SHT	OF
NONE	4	97

BOM Config

SYNC_MASTER=M51_DAVESYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

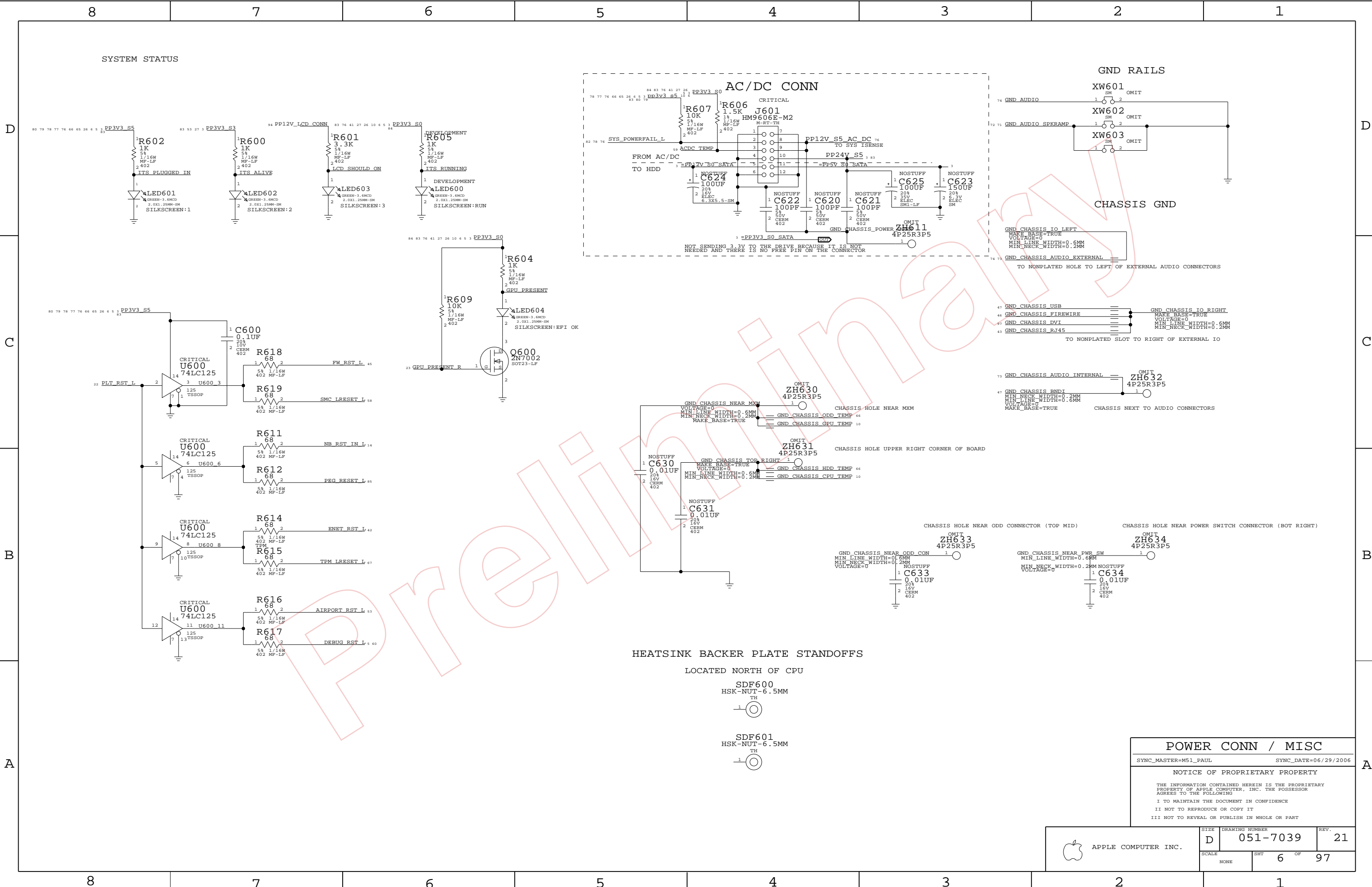
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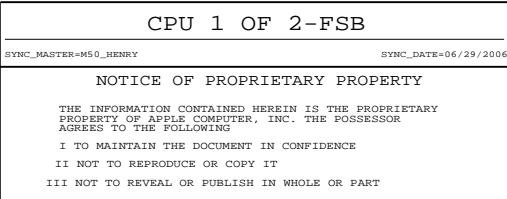
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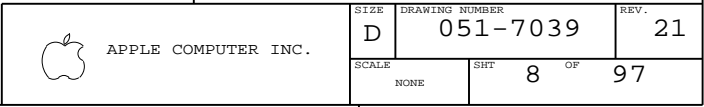


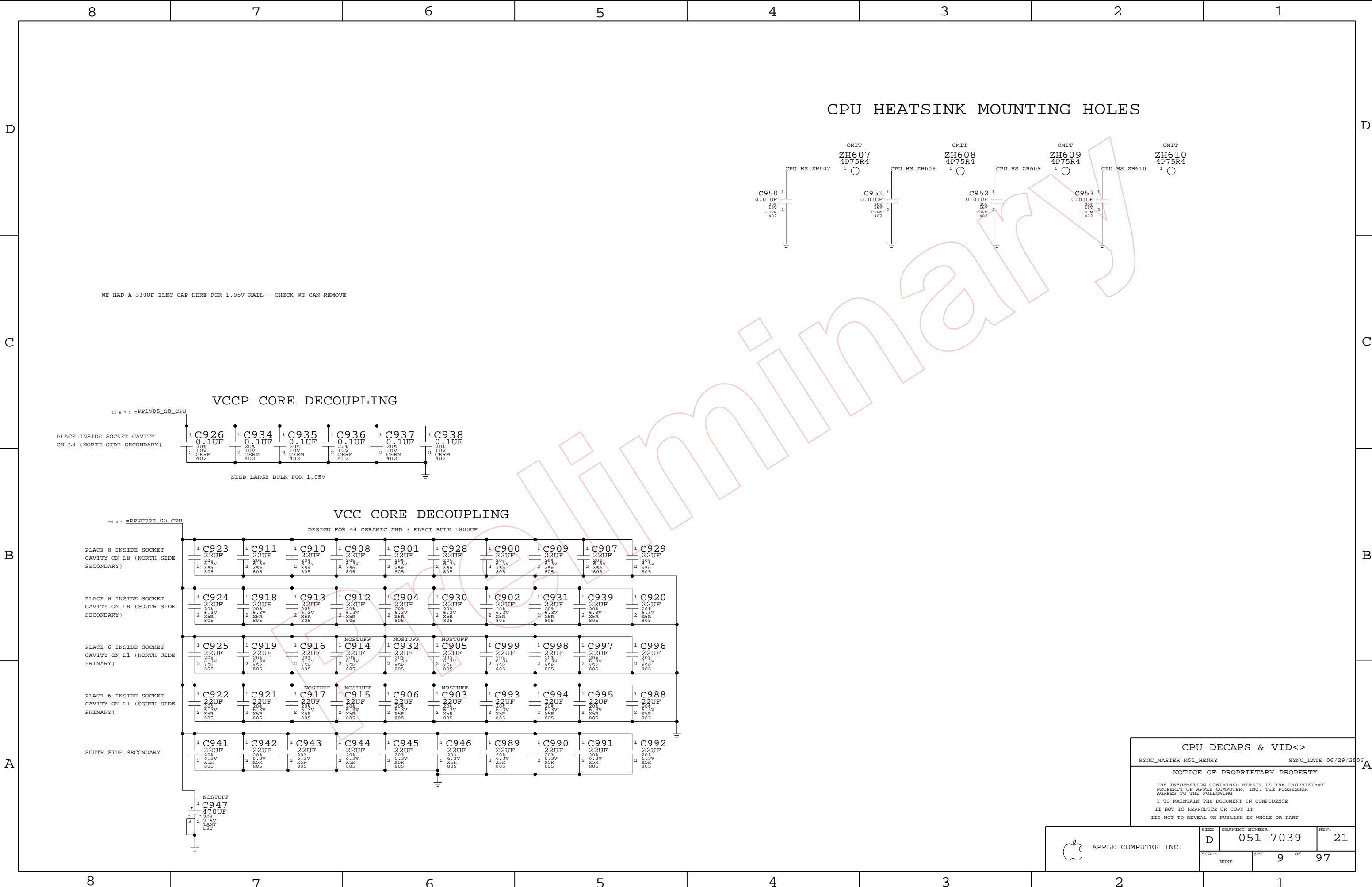


POWER CONN / MISC		
SYNC_MASTER=M51_PAUL		SYNC_DATE=06/29/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	21
SCALE		SHT	6 OF 97
NONE			







CPU DECAPS & VID<>

SYNC_MASTER=M51_HENRY

SYNC_DATE=06/29/2006


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	D	051-7039	21
SCALE		SHT	9 OF 97
NONE			

CPU ITP700FLEX DEBUG SUPPORT

DEVELOPMENT
J1101
52435-2872
P-RT-SM
29

11 9 8 7 3 =PP1V05 S0 CPU

1 R1101 54.9 1% 1/16W MF-LF 2 402

ITP R1103 54.9 1% 1/16W MF-LF 2 402

7 5 XDP TDO

ITP R1102 22.6 1% 1/16W MF-LF 2 402

(FROM CK410M HOST 133/167MHZ)

12 7 5 FSB CPURST L

ITP R1100 22.6 1% 1/16W MF-LF 2 402

23 3 =PP3V3 S5 SB PM

ITP R1104 240 5% 1/16W MF-LF 2 402

E7 HAS OTHER PULL UP RESISTORS THAT MAY IMPACT ITP FUNCTIONALITY

(AND WITH RESET BUTTON)

26 7 5 XDP DBRESET L

11 9 8 7 3 =PP1V05 S0 CPU

ITP C1100 0.1UF 10% 195 2 402

ITP R1106 680 5% 1/16W MF-LF 2 402

518S0320

1 XDP TDI

2 XDP TMS

3 XDP TRST L

4 XDP TCK (TCK)

5 XDP TCK (FBO)

6 XDP TDO

7 CPU XDP CLK N

8 CPU XDP CLK P

9 XDP TCK (FBO)

10 ITPRESET L

11 XDP BPM L<5>

12 XDP BPM L<4>

13 XDP BPM L<3>

14 XDP BPM L<2>

15 XDP BPM L<1>

16 XDP BPM L<0>

17 NC

18 NC

19 NC

20 NC

21 NC

22 NC

23 NC

24 NC

25 NC

26 NC

27 NC

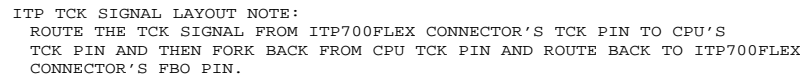
28 NC

29 NC

DBA#1 INDICATE THAT I (DEBUG PORT ACTIVE)

DBR#1 TO ICH7M SYS_RST (DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.



```

CPU ITP700FLEX  DEBUG
SYNC_MASTER=M50_HENRY      SYNC_DATE=06/29/2006

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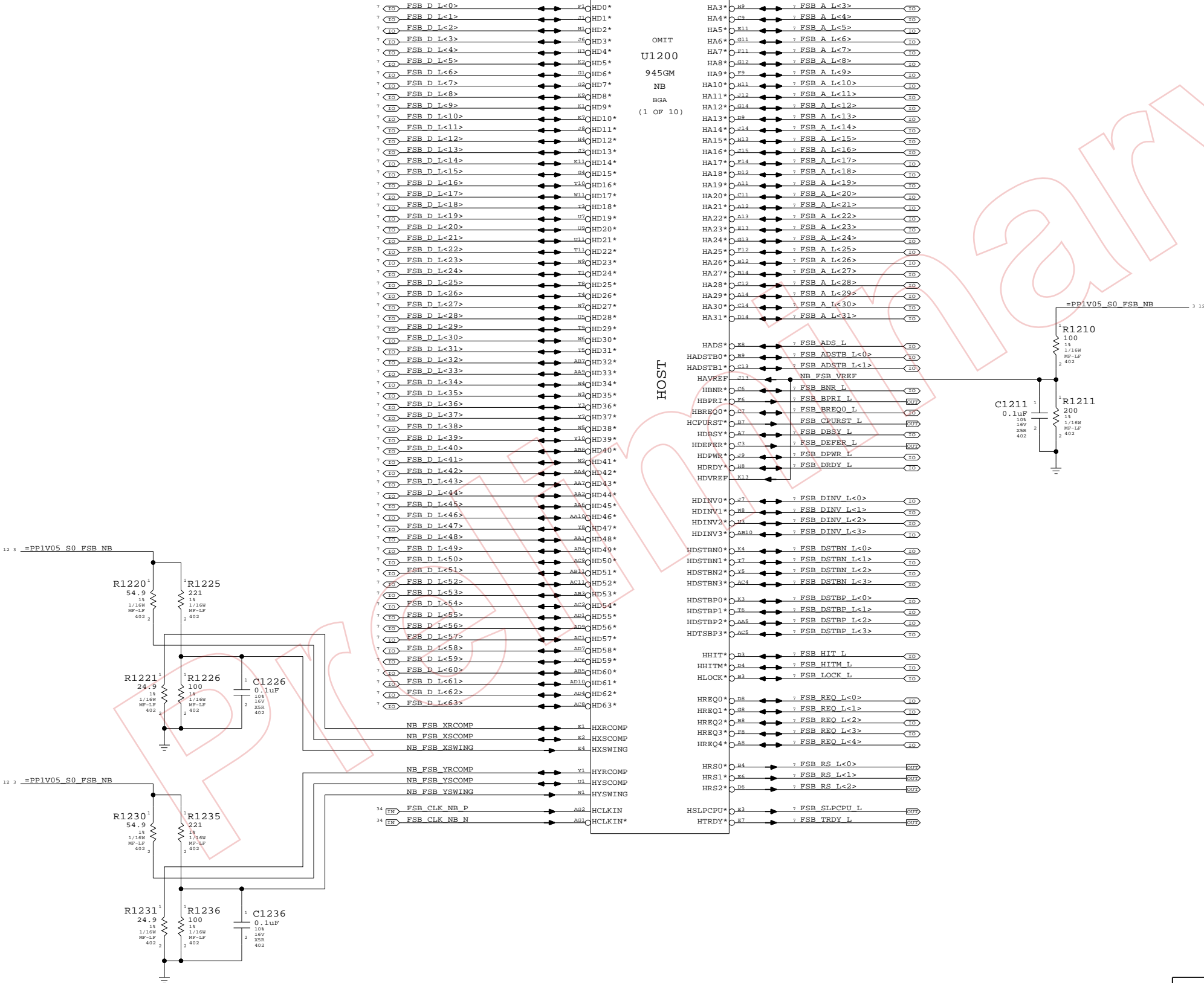
A

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A



NB CPU Interface

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

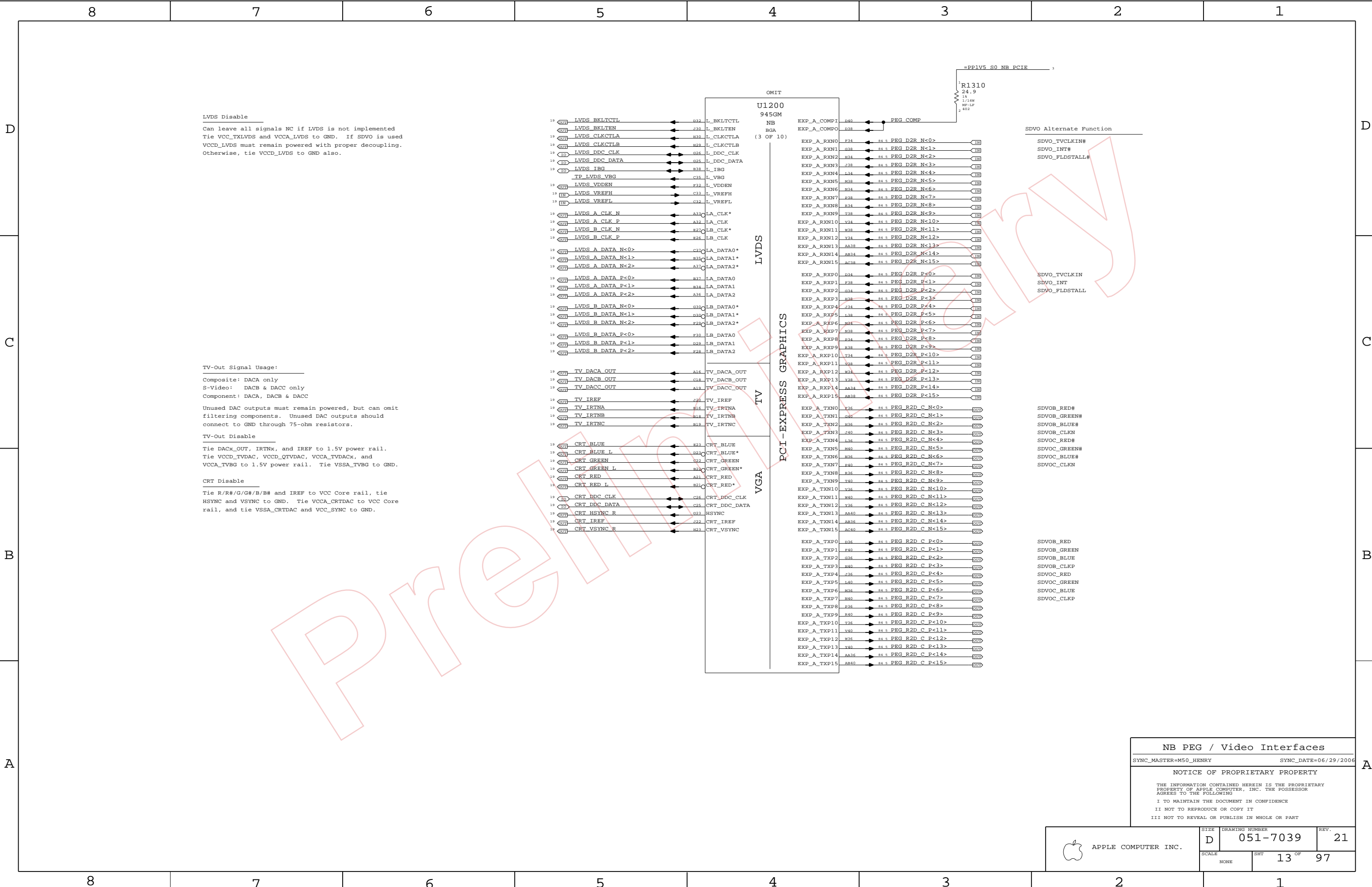
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LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
filtering components. Unused DAC outputs should
connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

NB PEG / Video Interfaces

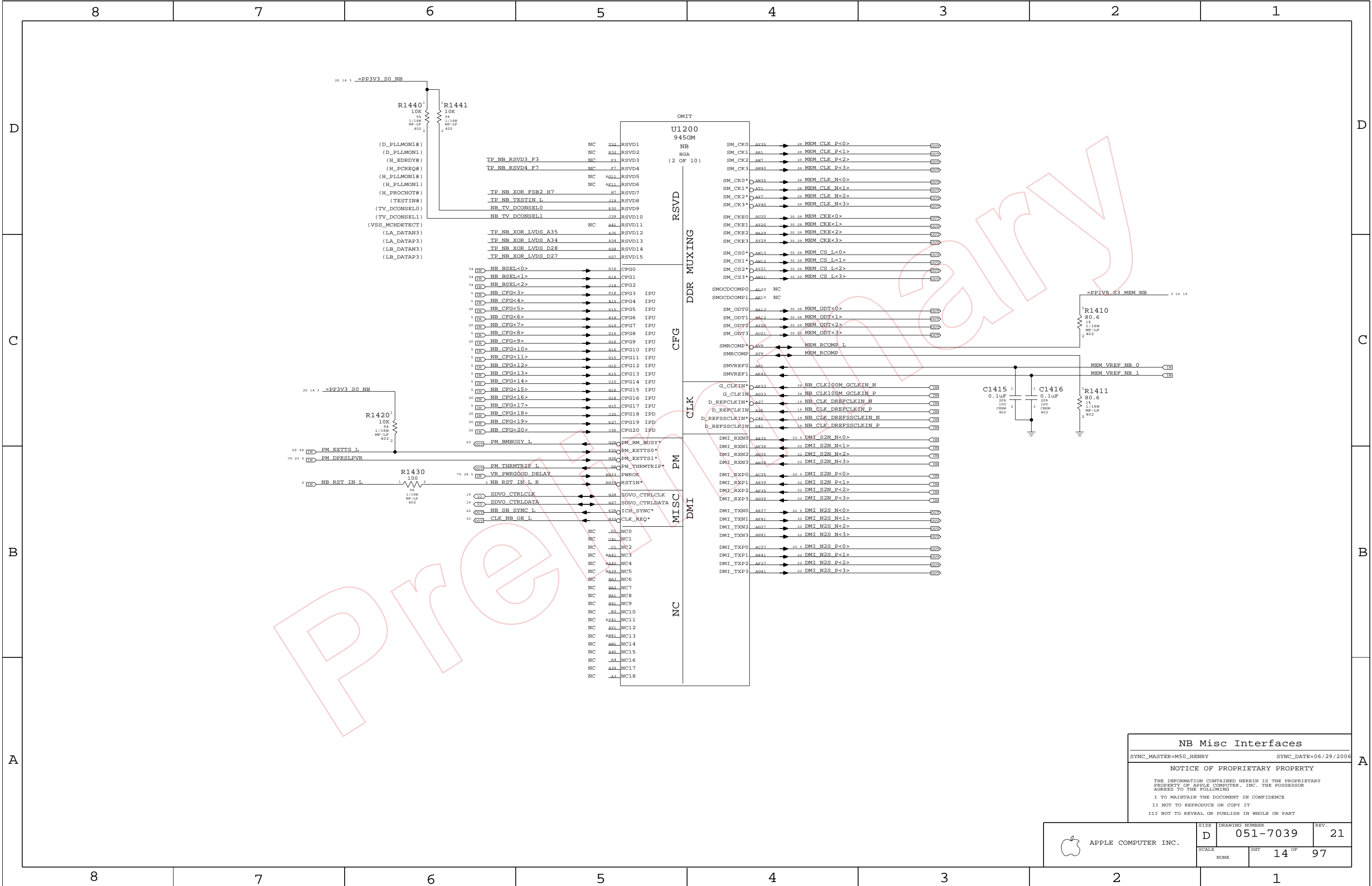
SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. 21
	SCALE NONE	SHT 13 OF 97	



NB Misc Interfaces

SYNC_MASTER=M50_HENRY

SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

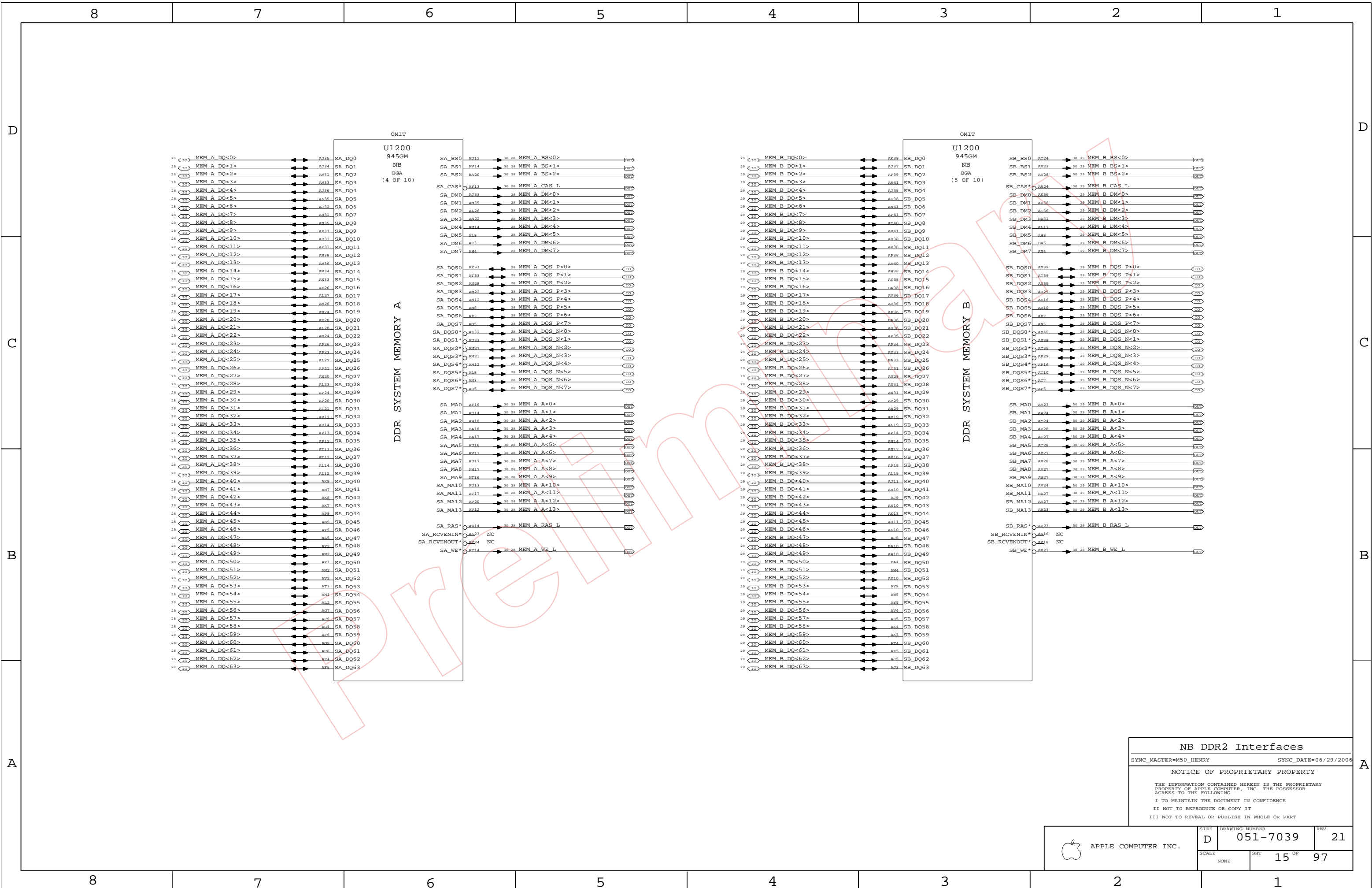
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	D	051-7039	21
SCALE		SHT	14 OF 97
NONE			



NB DDR2 Interfaces

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

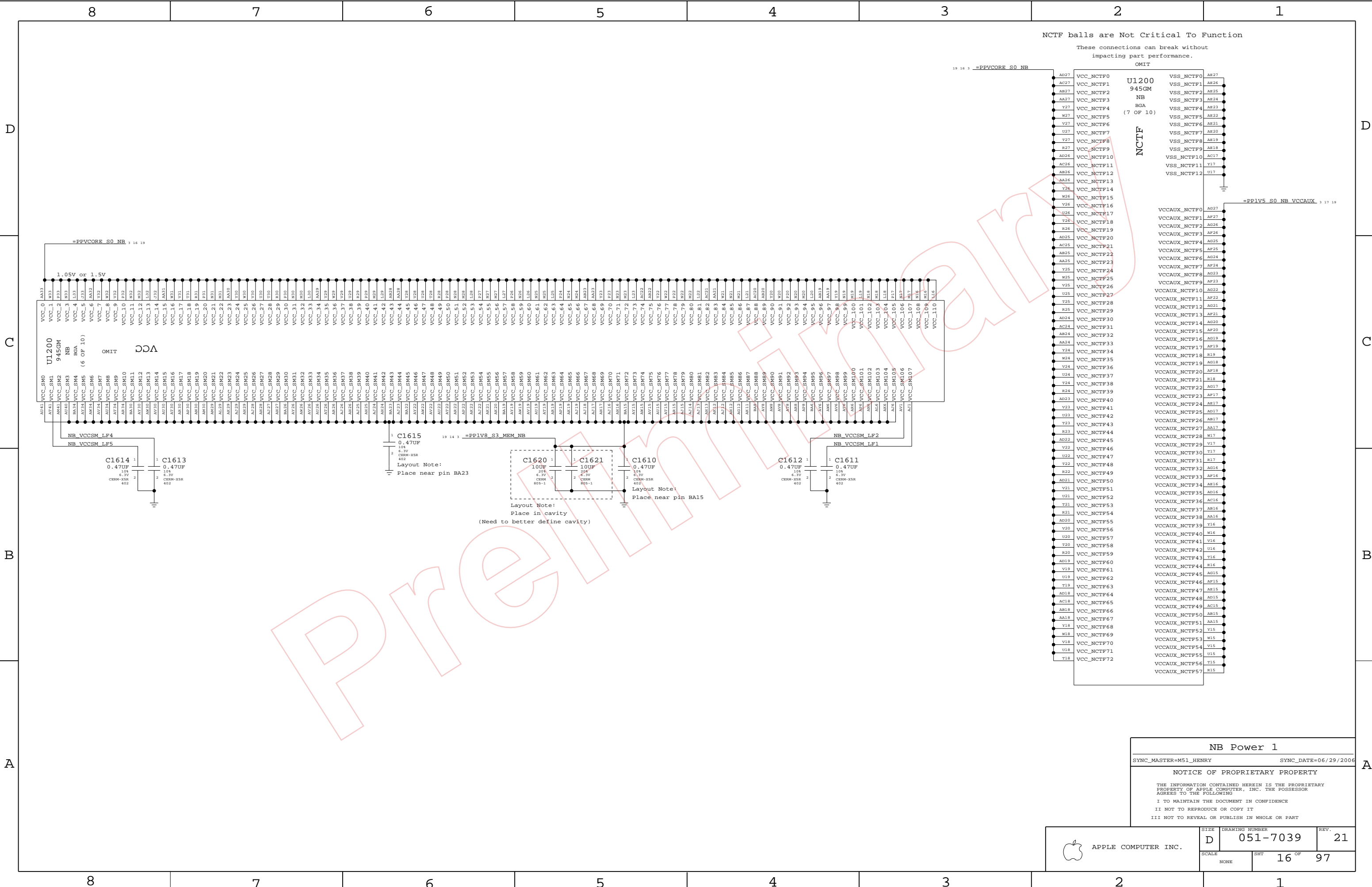
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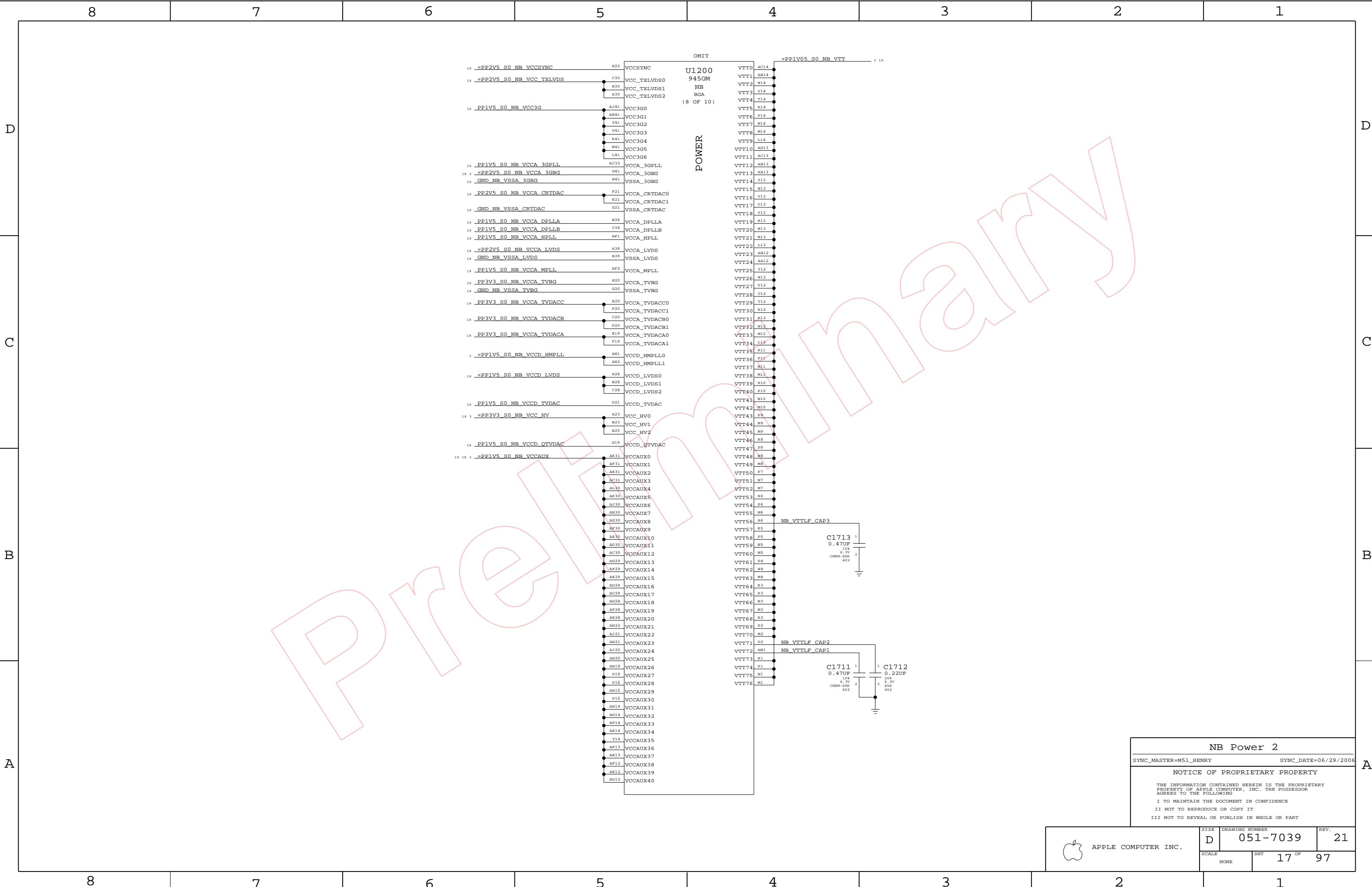
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NB Power 2

SYNC_MASTER=M51_HENRY

SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

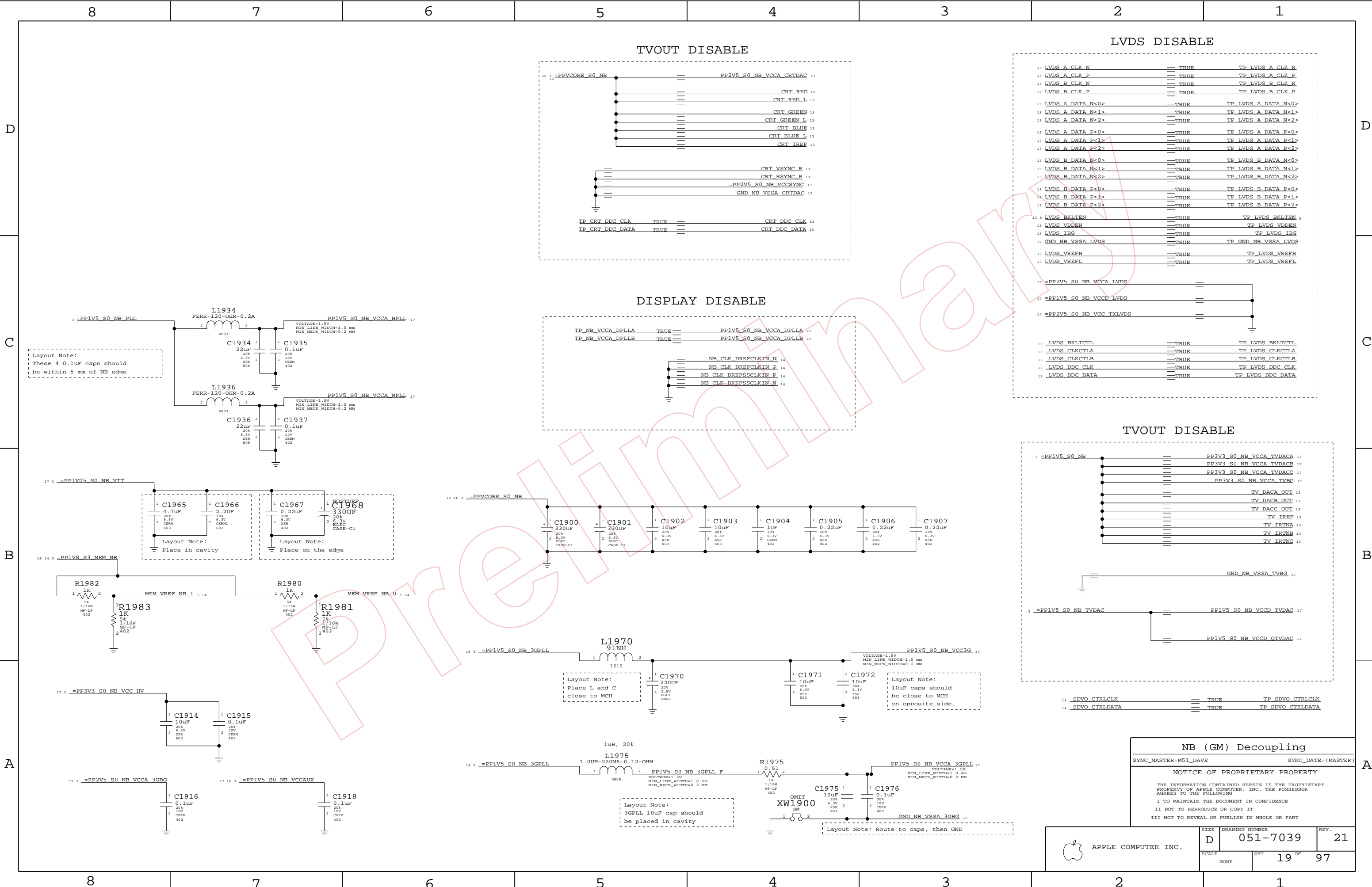
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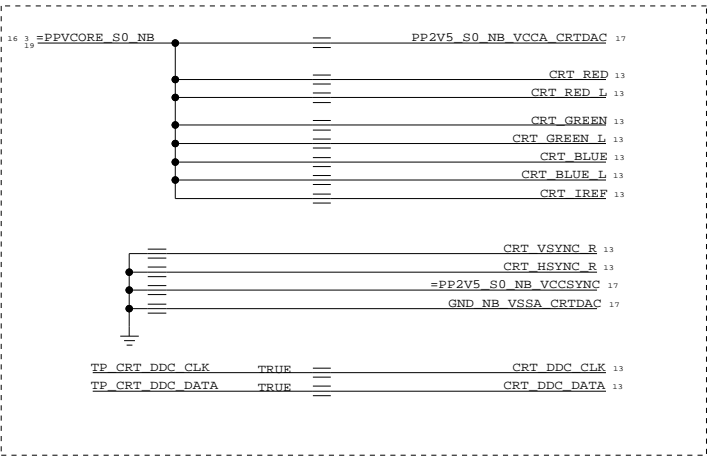
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

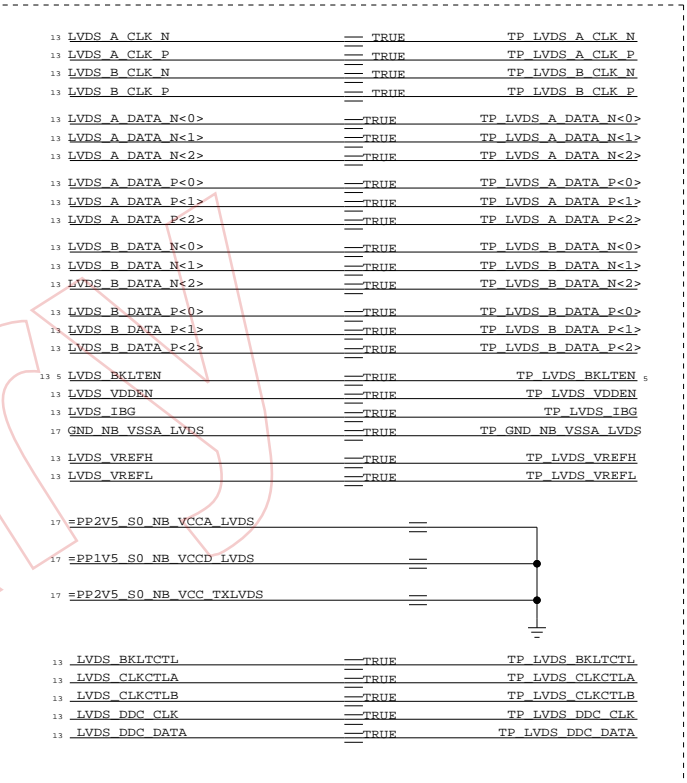
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	21
SCALE		SHT	17 OF 97
NONE			



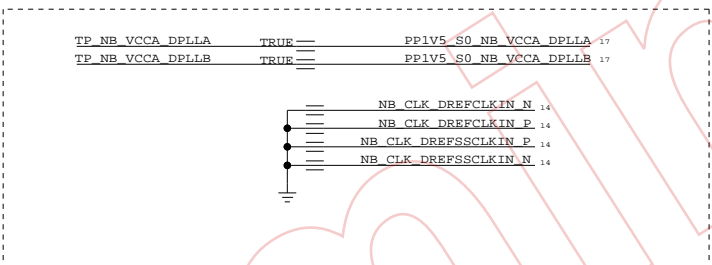
TVOUT DISABLE



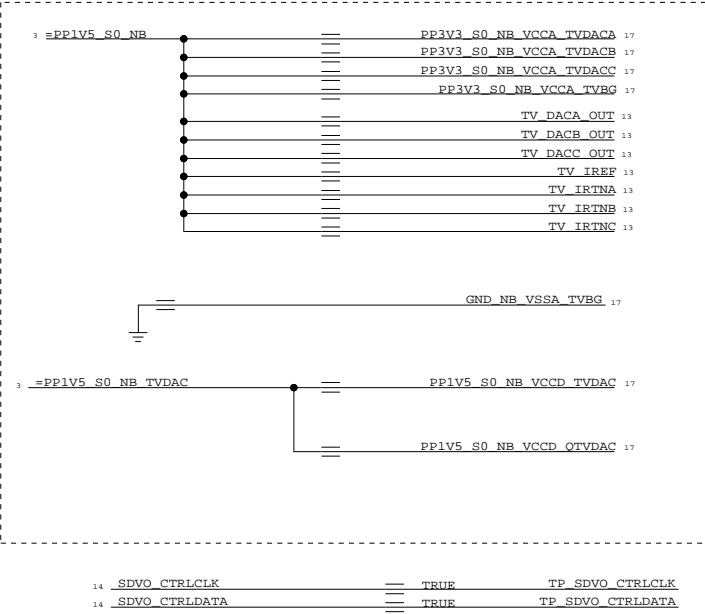
LVDS DISABLE



DISPLAY DISABLE

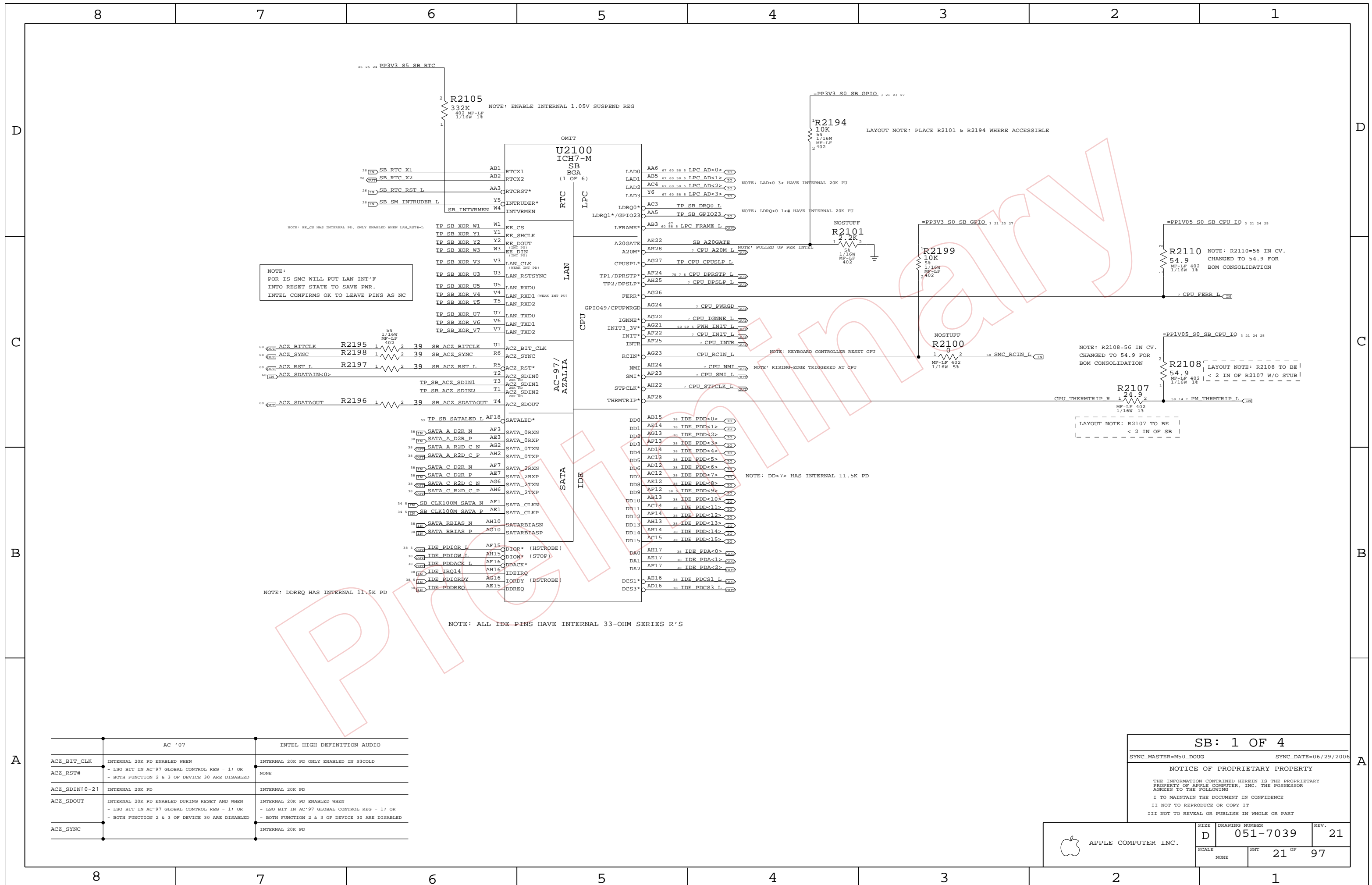


TVOUT DISABLE

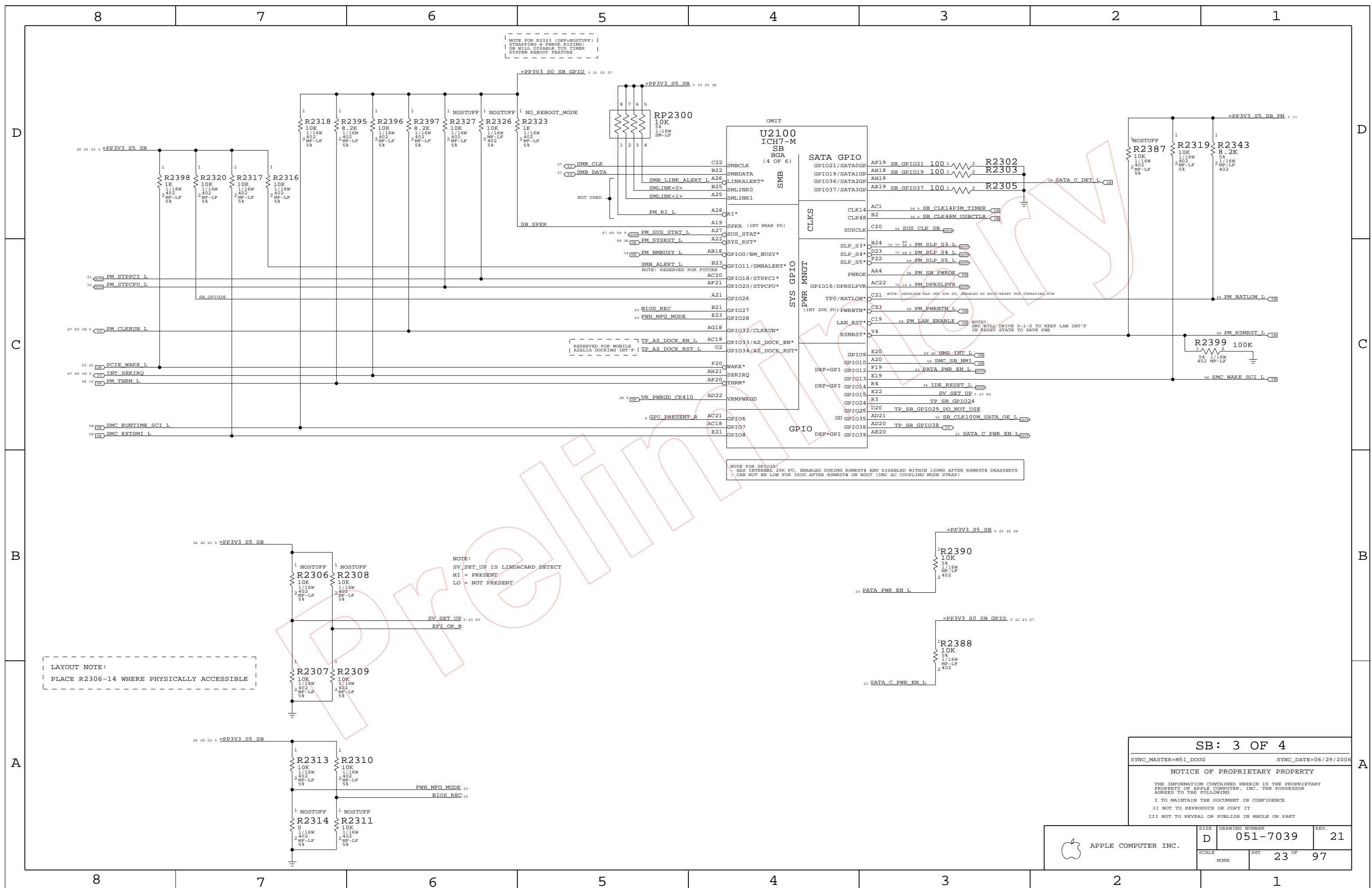


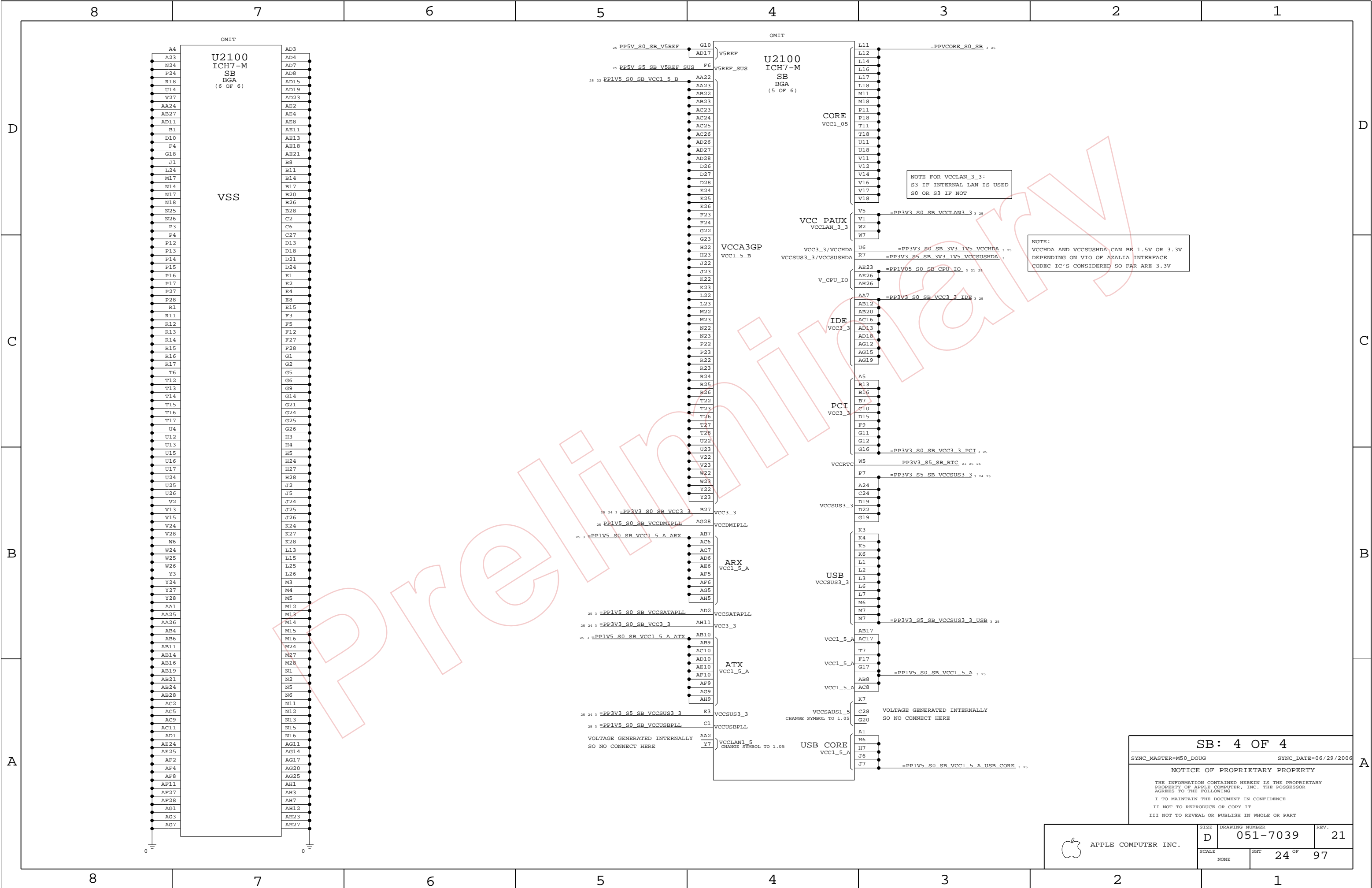
NB (GM) Decoupling	
SYNC_MASTER=M51_DAVE	SYNC_DATE=(MASTER)
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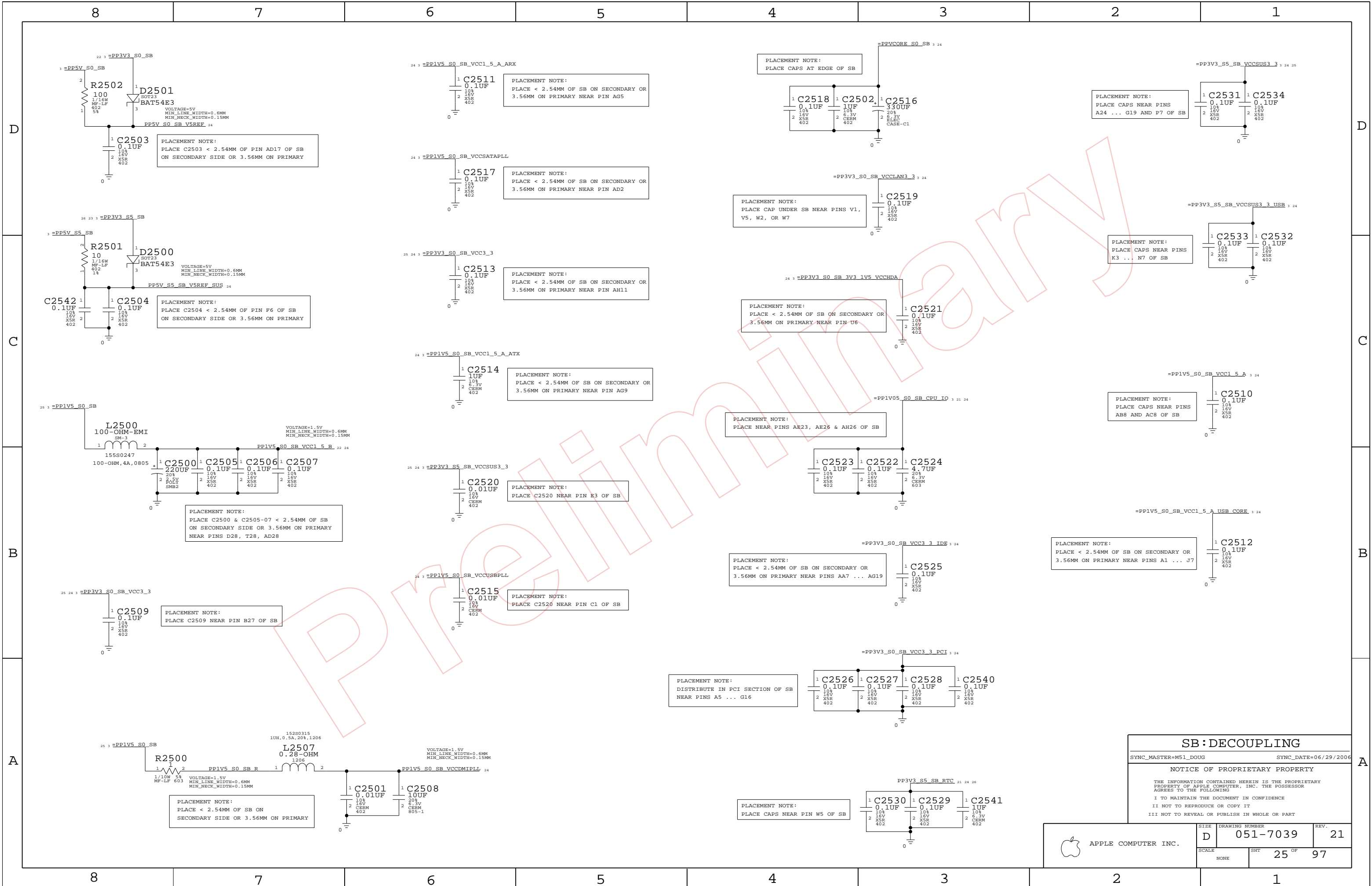
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	21
SCALE		SHT	19 OF 97
NONE			



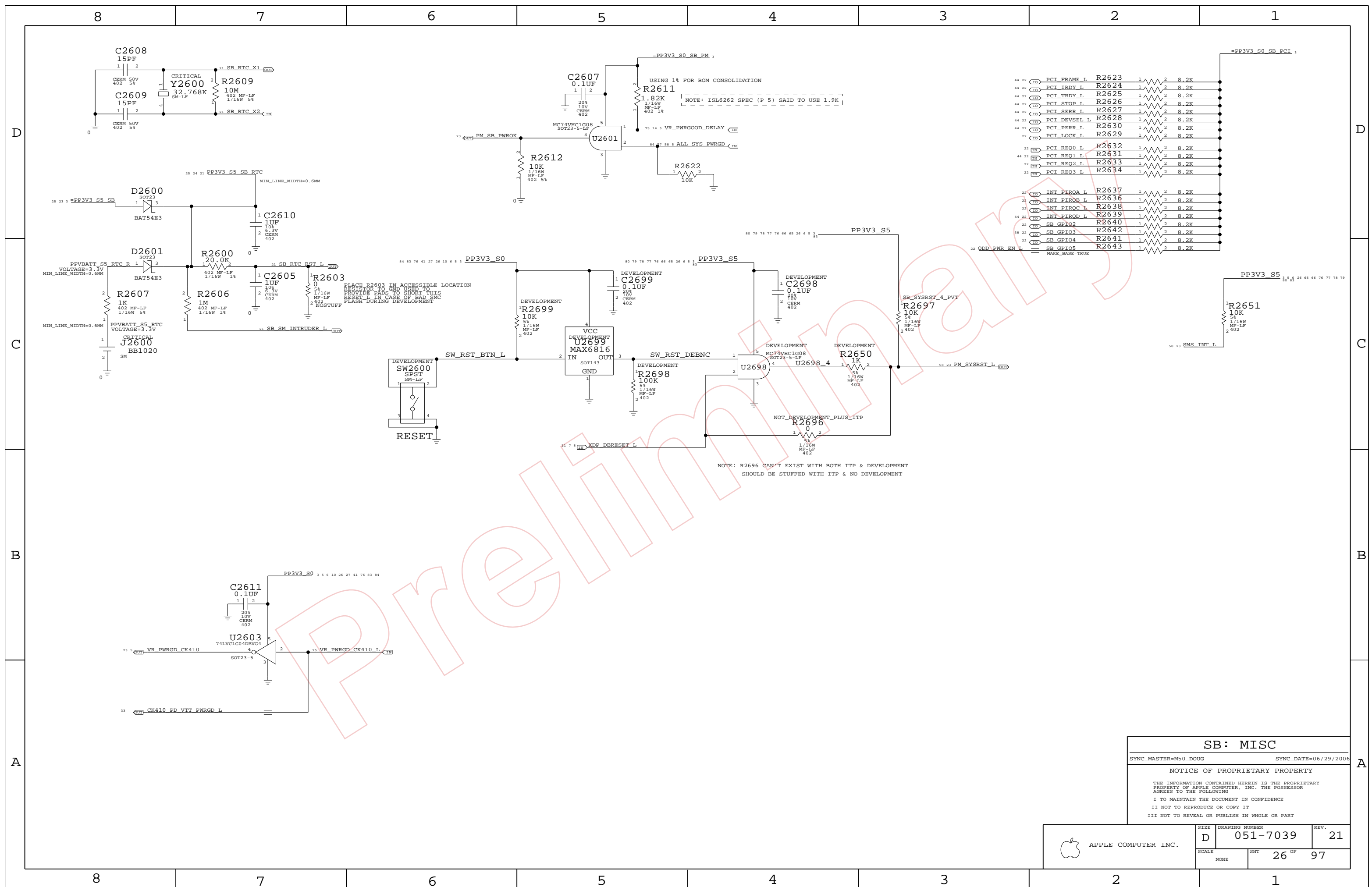


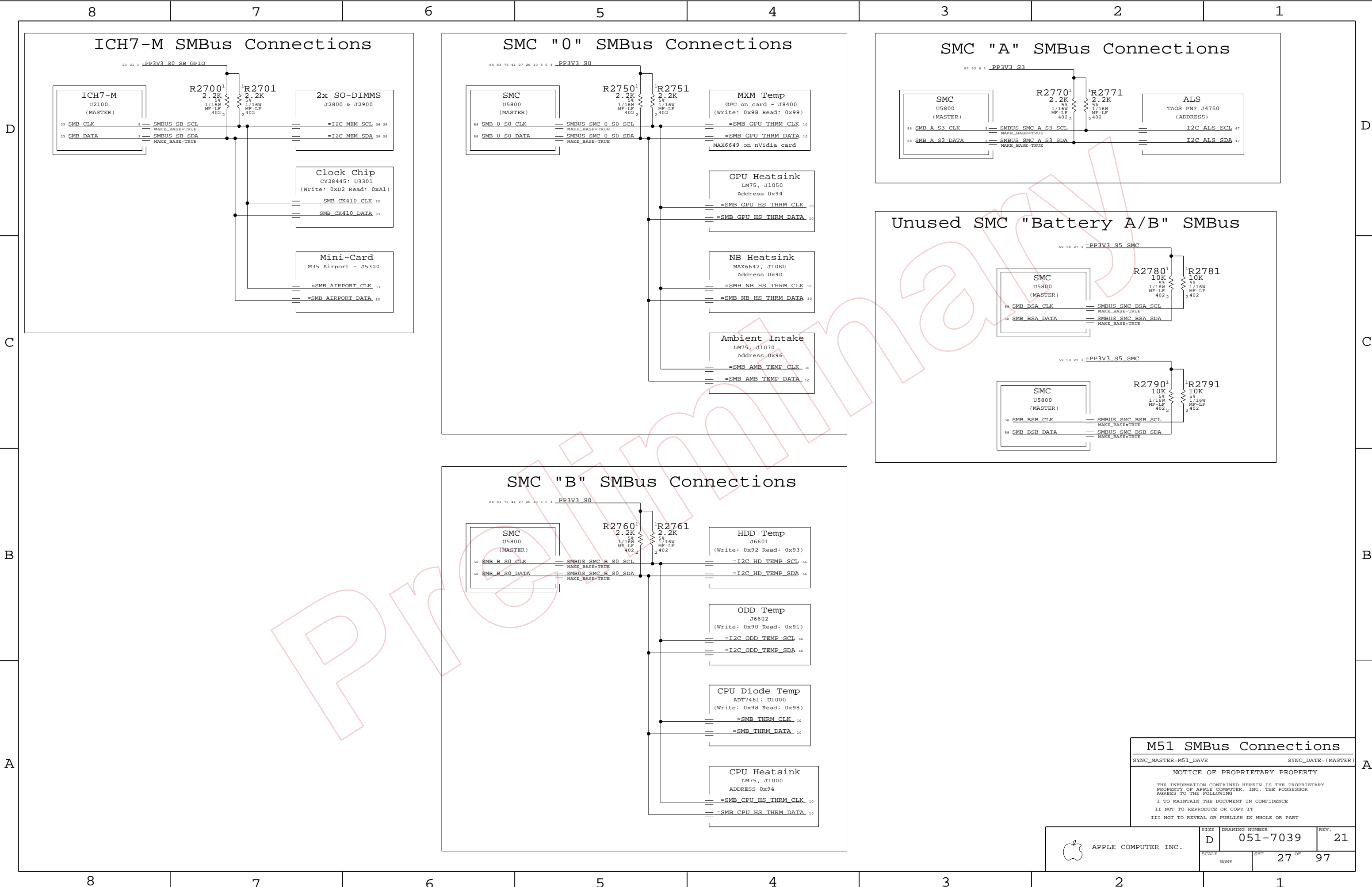






SB: DECOUPLING		
SYNC_MASTER=M51_D0UG		SYNC_DATE=06/29/2006
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SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE	SHT	25 OF 97
NONE		





Page Notes

Power aliases required by this page:

- =P1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:

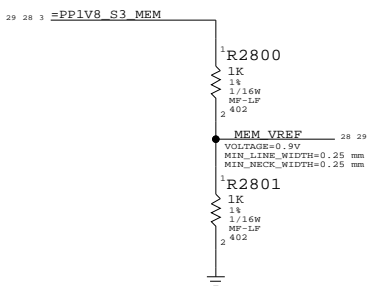
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:

(NONE)

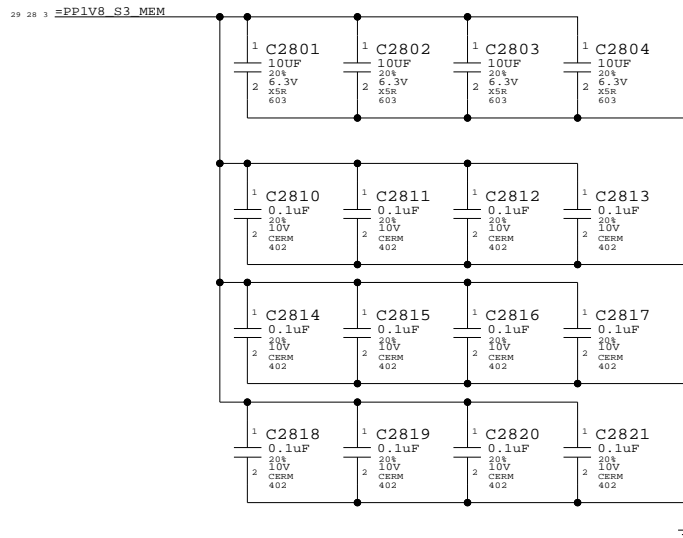
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

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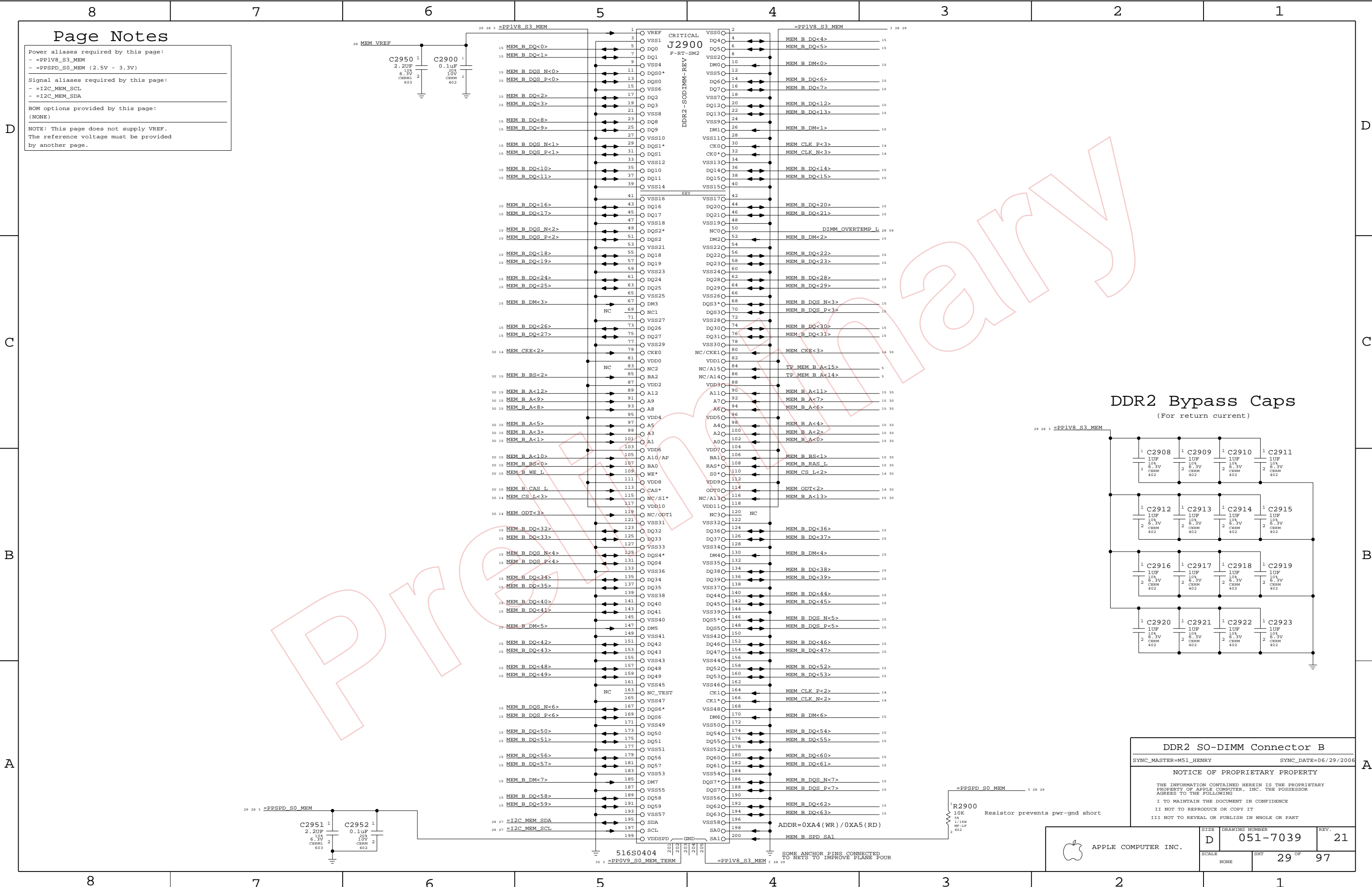
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APPLE COMPUTER INC.

SIZE D DRAWING NUMBER 051-7039 REV. 21

SCALE NONE SHT 28 OF 97



Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

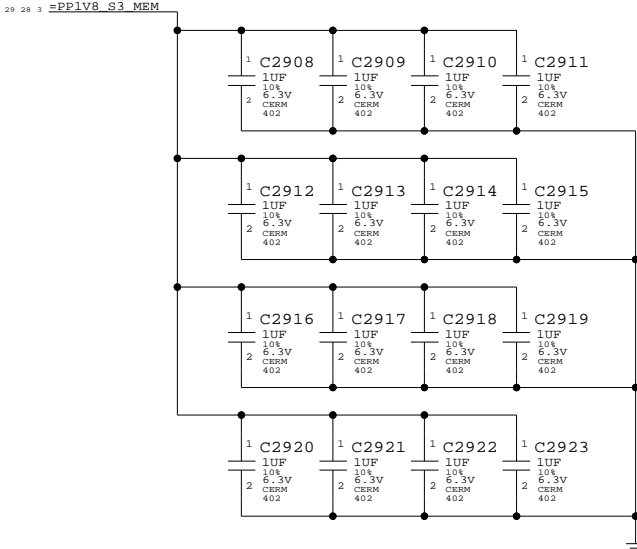
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B

SYNC_MASTER=M51_HENRY

SYNC_DATE=06/29/2006

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APPLE COMPUTER INC.

SIZE D

DRAWING NUMBER 051-7039

REV. 21

SCALE NONE

SHT 29

OF 97

=PPSPD_S0_MEM

R2900

10K

5% 1/16W NF-1P

2 402

Resistor prevents pwr-gnd short

SOME ANCHOR PINS CONNECTED TO NETS TO IMPROVE PLANE POUR

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

D

C

B

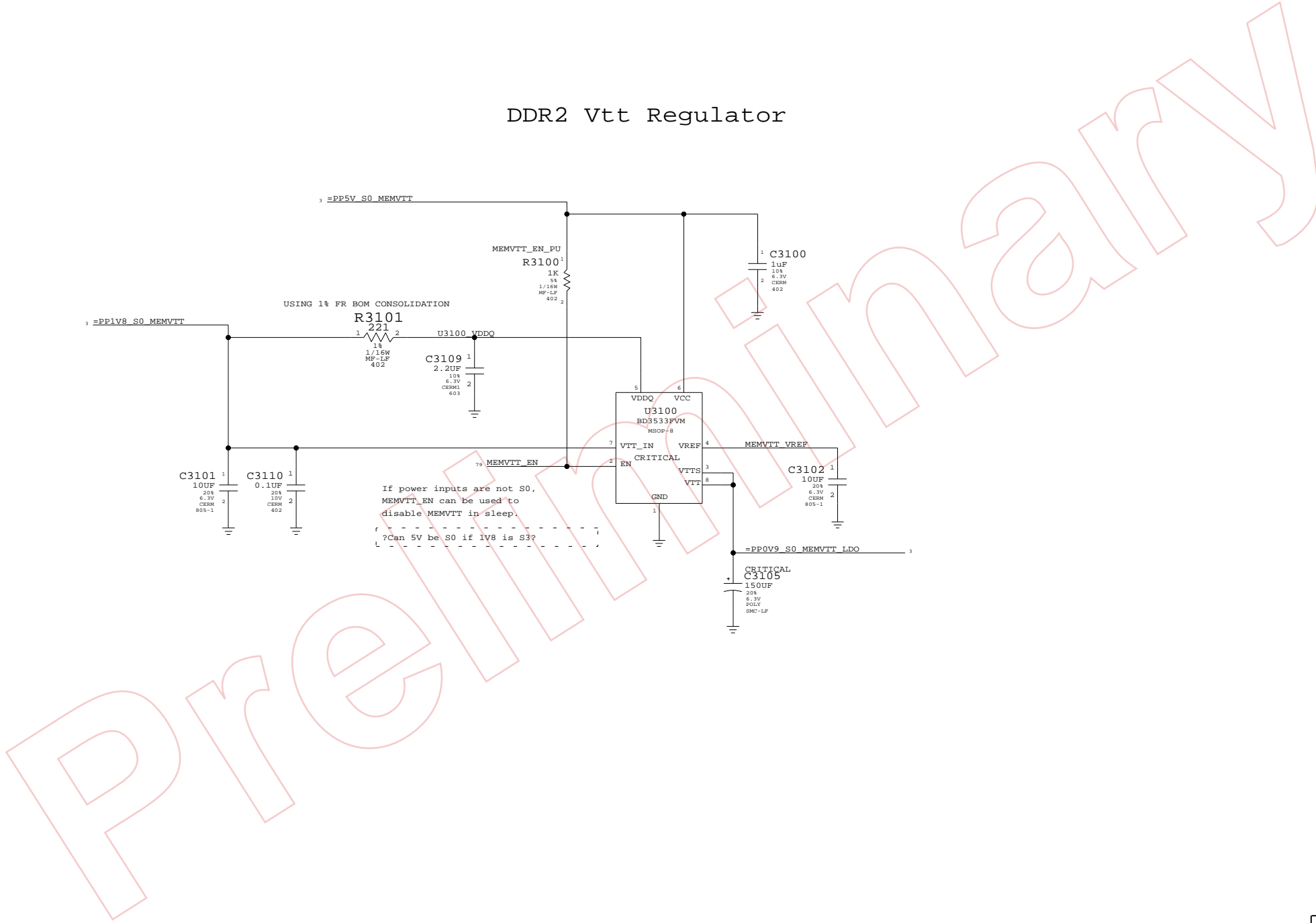
A

D

C

B

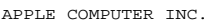
A



SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

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DRAWING NUMBER

051-7039

25

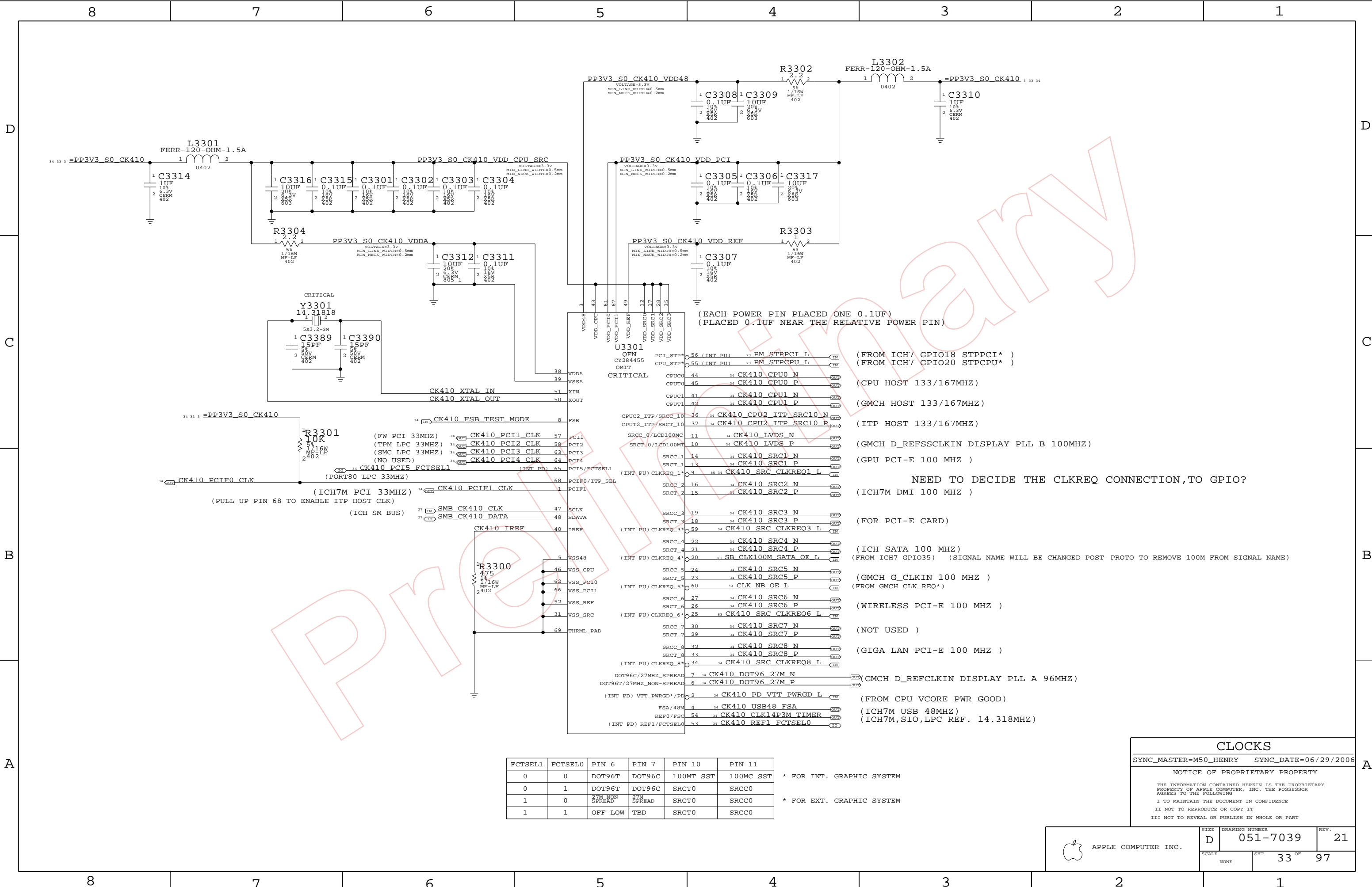
[illegible]

SHT 31 OF 05

SHT 31 OF 05

NONE

31 9



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM

* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=M50_HENRY SYNC_DATE=06/29/2006

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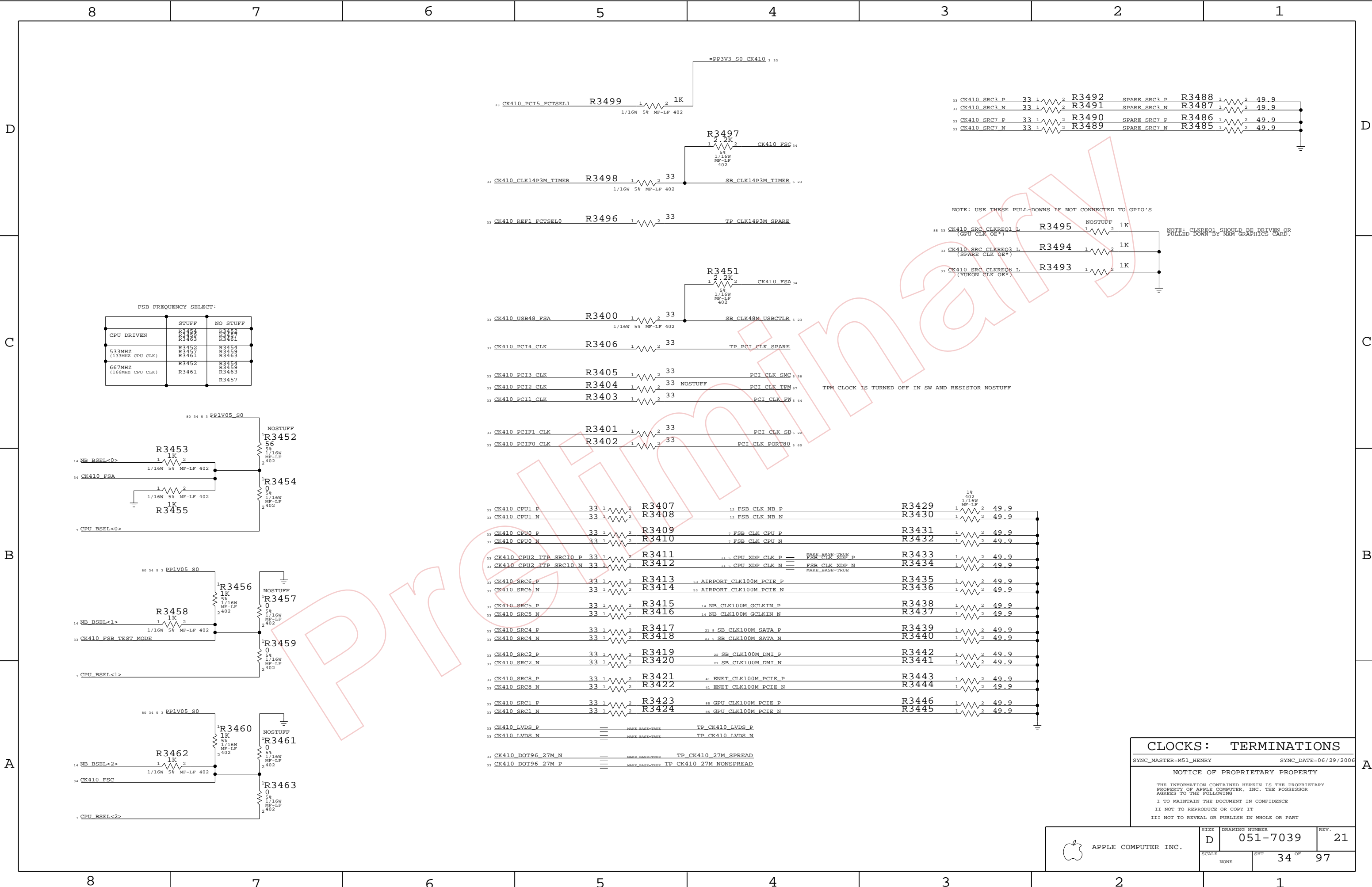
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SIZE D DRAWING NUMBER 051-7039 REV. 21

SCALE NONE SHT 33 OF 97



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3454 R3455 R3456	R3457 R3458 R3459
533MHZ (133MHZ CPU CLK)	R3452 R3453 R3454	R3455 R3456 R3457
667MHZ (166MHZ CPU CLK)	R3452 R3453 R3454	R3455 R3456 R3457

CLOCKS: TERMINATIONS

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

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SIZE D DRAWING NUMBER 051-7039 REV. 21

SCALE NONE SHT 34 OF 97

D

C

B

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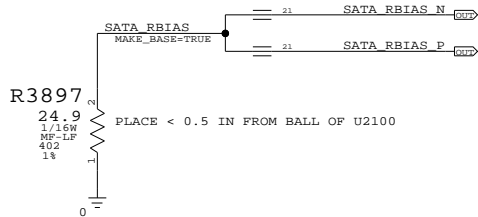
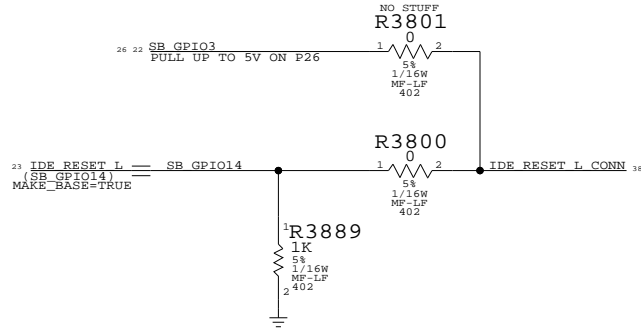
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C

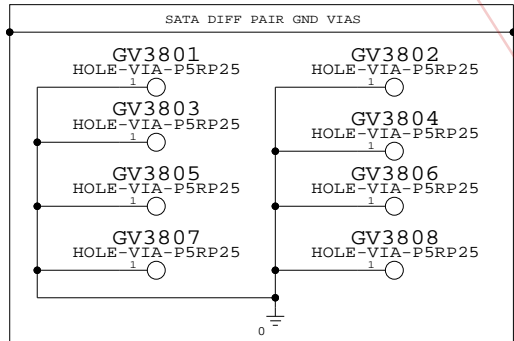
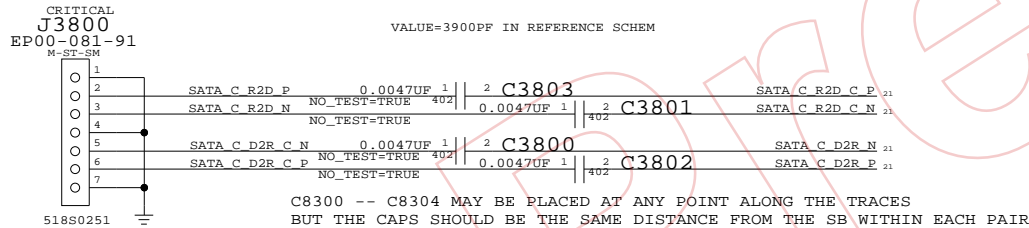
B

A

PATA (ODD) CONNECTOR



SATA CONNECTOR



SATA PORT 0 IS NOT USED

SATA A R2D C P

TP SATA A R2D P

MAKE_BASE=TRUE

SATA A R2D C N

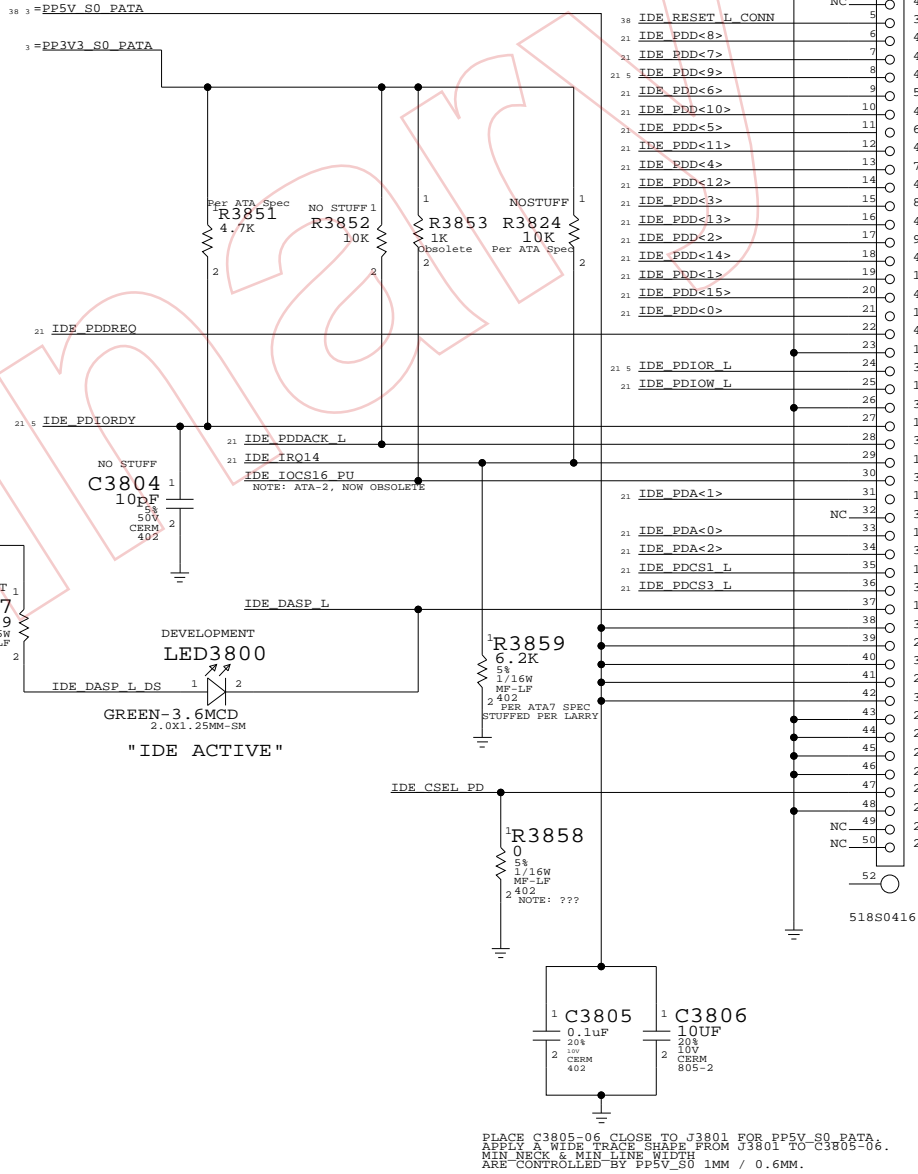
TP SATA A R2D N

MAKE_BASE=TRUE

SATA A D2R P

MAKE_BASE=TRUE

SATA A D2R N

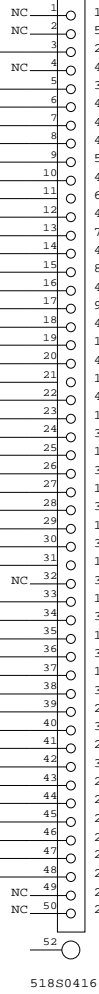


CRITICAL

J3801

87151-5005N

P-RT-SM



Disk Connectors

SYNC_MASTER=M51_D0UG

SYNC_DATE=06/29/2006

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SIZE

DRAWING NUMBER

REV.

D

051-7039

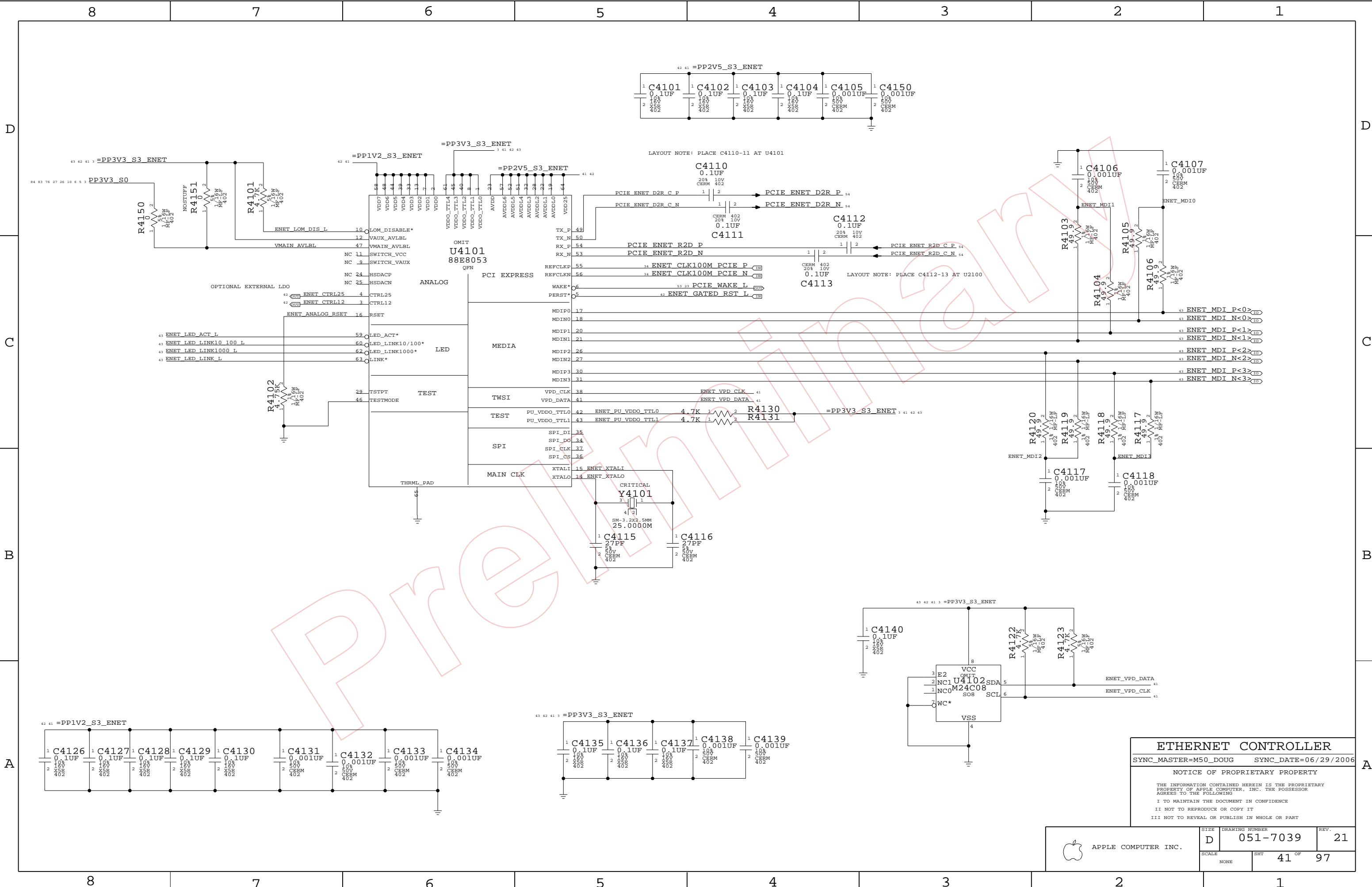
21

SCALE

NONE

SHT

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ETHERNET CONTROLLER
SYNC_MASTER=M50_DOUG SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

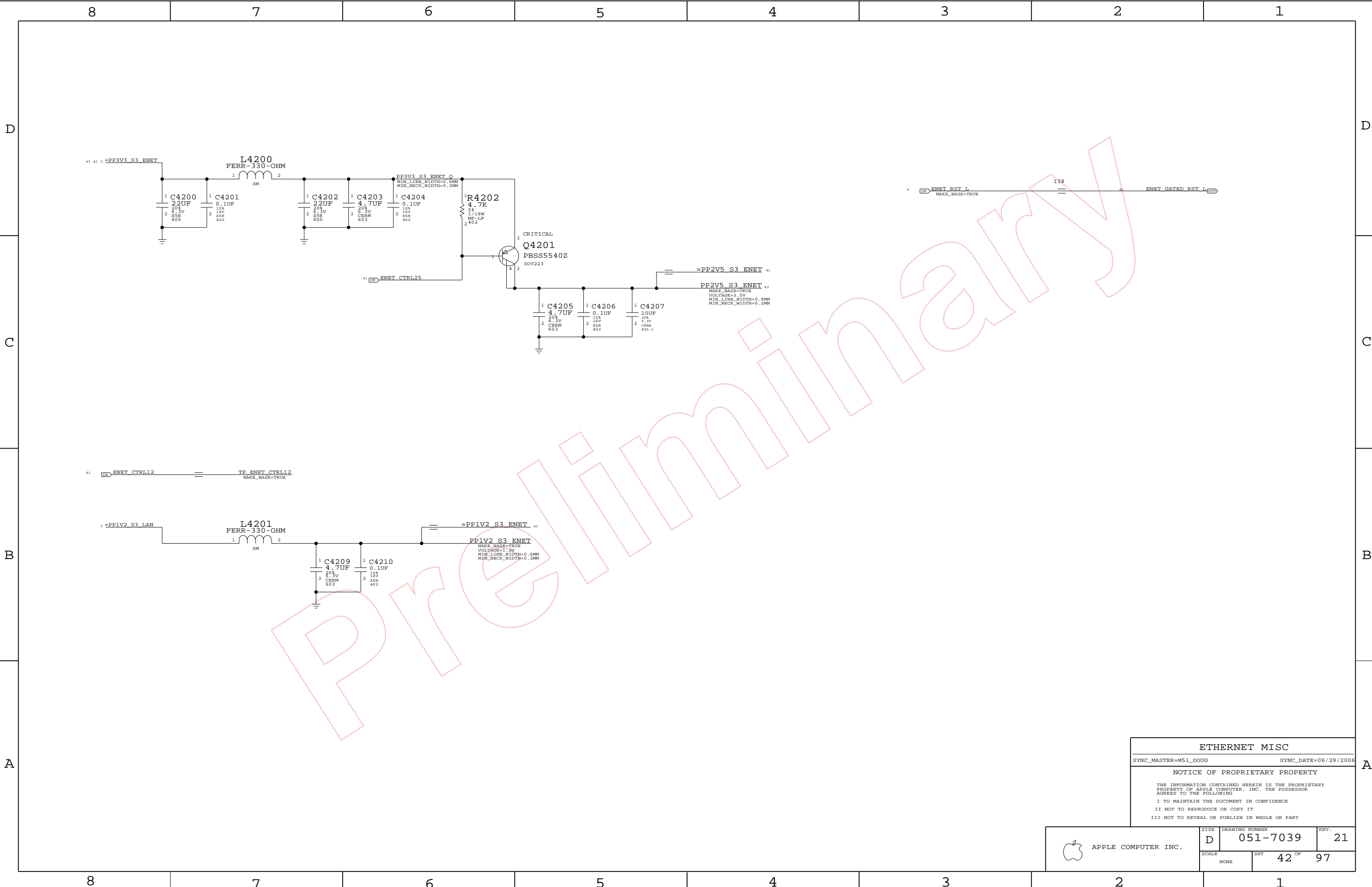
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	D	051-7039	21
SCALE		SHT	41 OF 97
NONE			



ETHERNET MISC

SYNC_MASTER=M51_DOUG SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

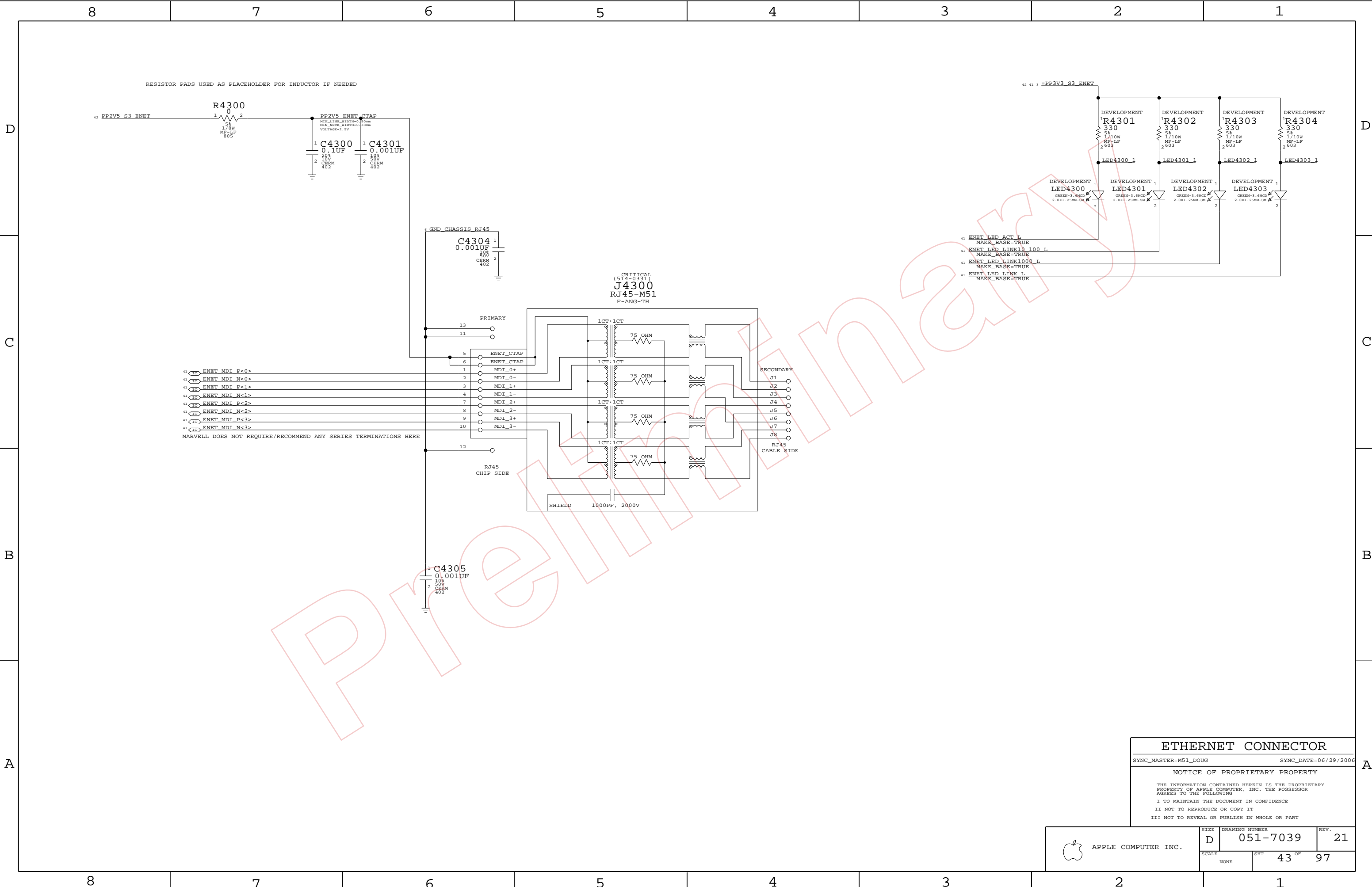
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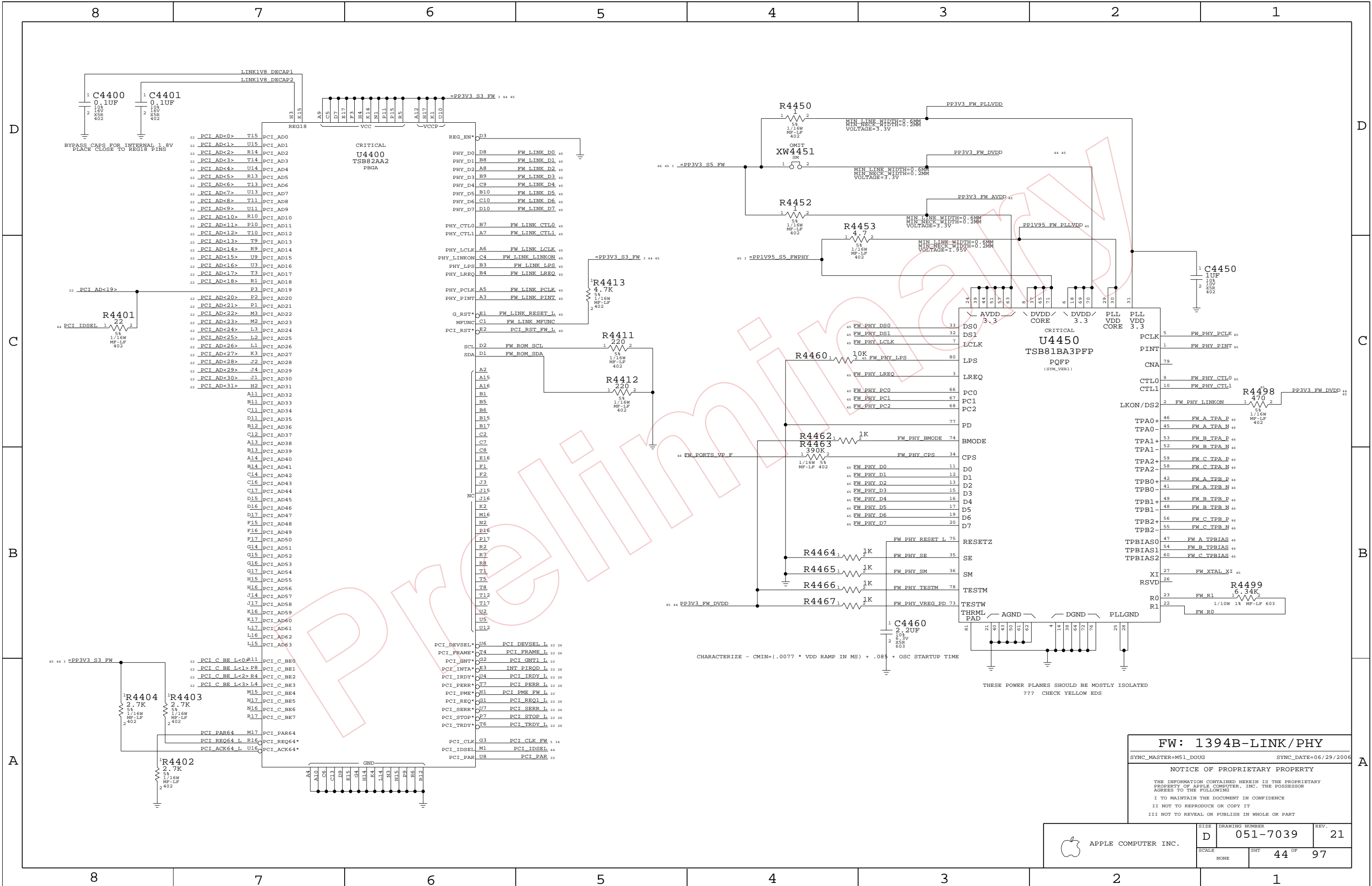
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

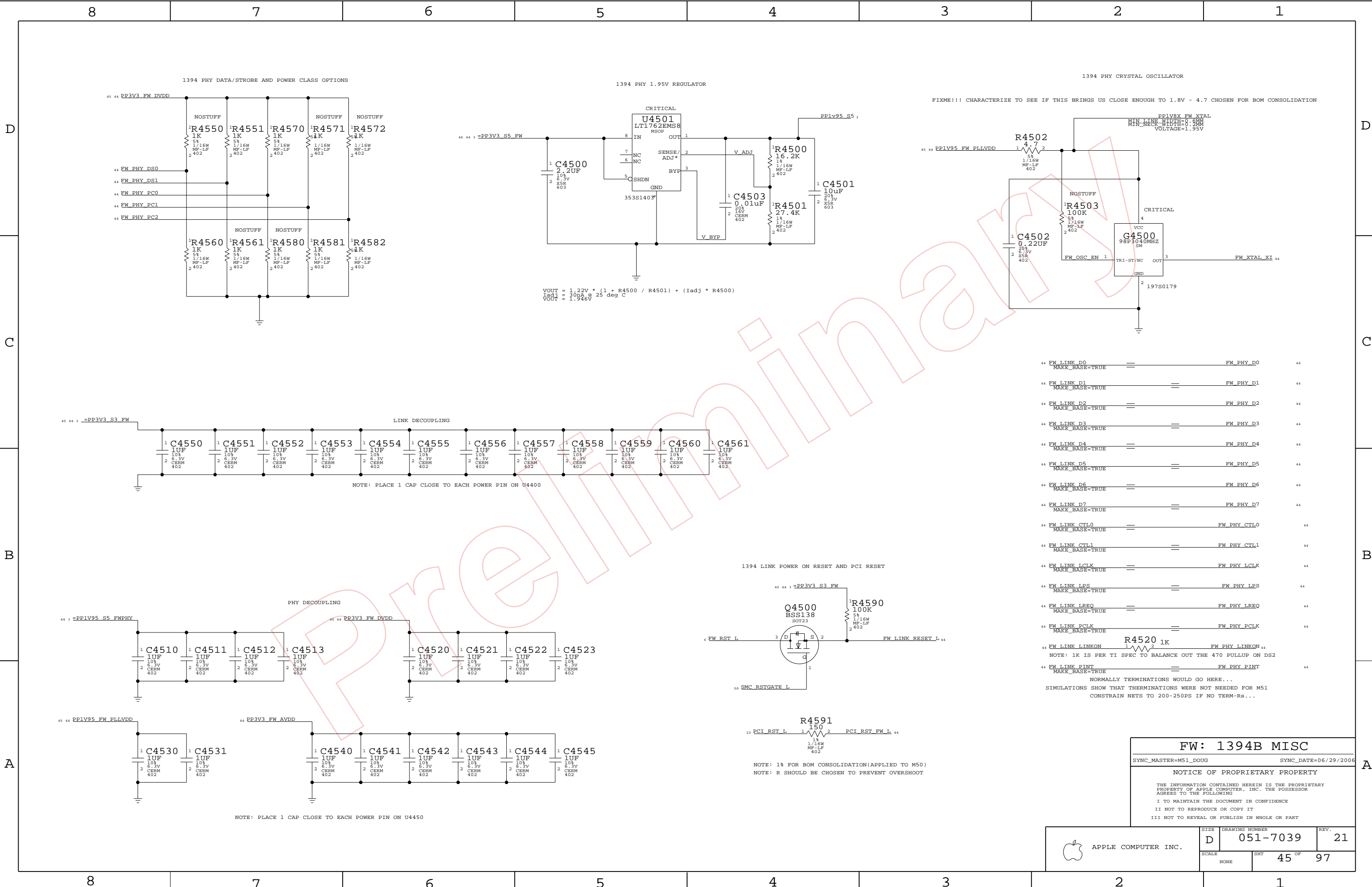
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	21
SCALE		SHT	42 OF 97
NONE			

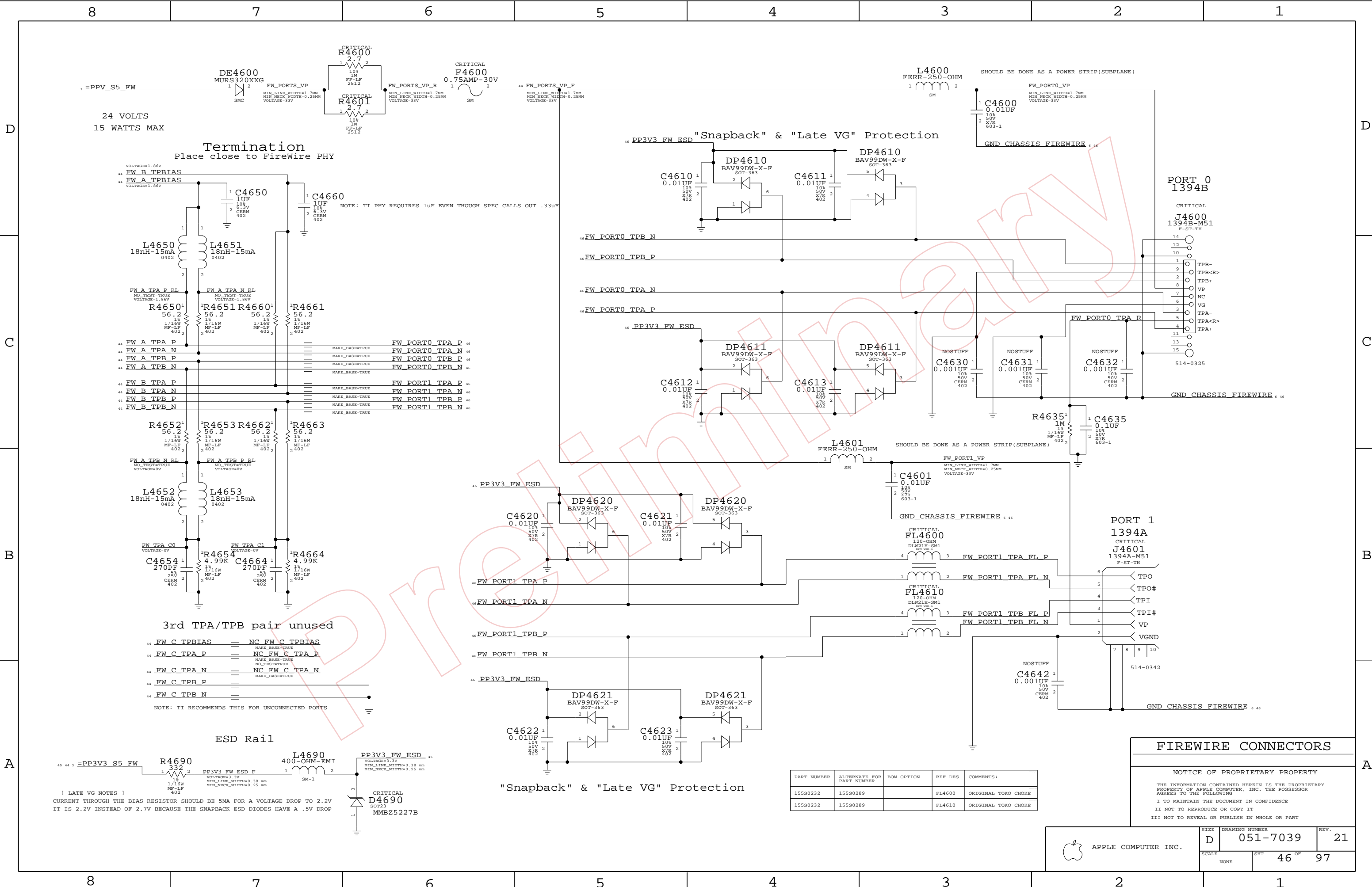


ETHERNET CONNECTOR	
SYNC_MASTER=M51_DOUG	SYNC_DATE=06/29/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. 21
	SCALE NONE	SHT 43 OF 97	







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4600	ORIGINAL TOKO CHOKE
155S0232	155S0289		FL4610	ORIGINAL TOKO CHOKE

FIREWIRE CONNECTORS

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APPLE COMPUTER INC.

SIZE

D

DRAWING NUMBER

051-7039

REV.

21

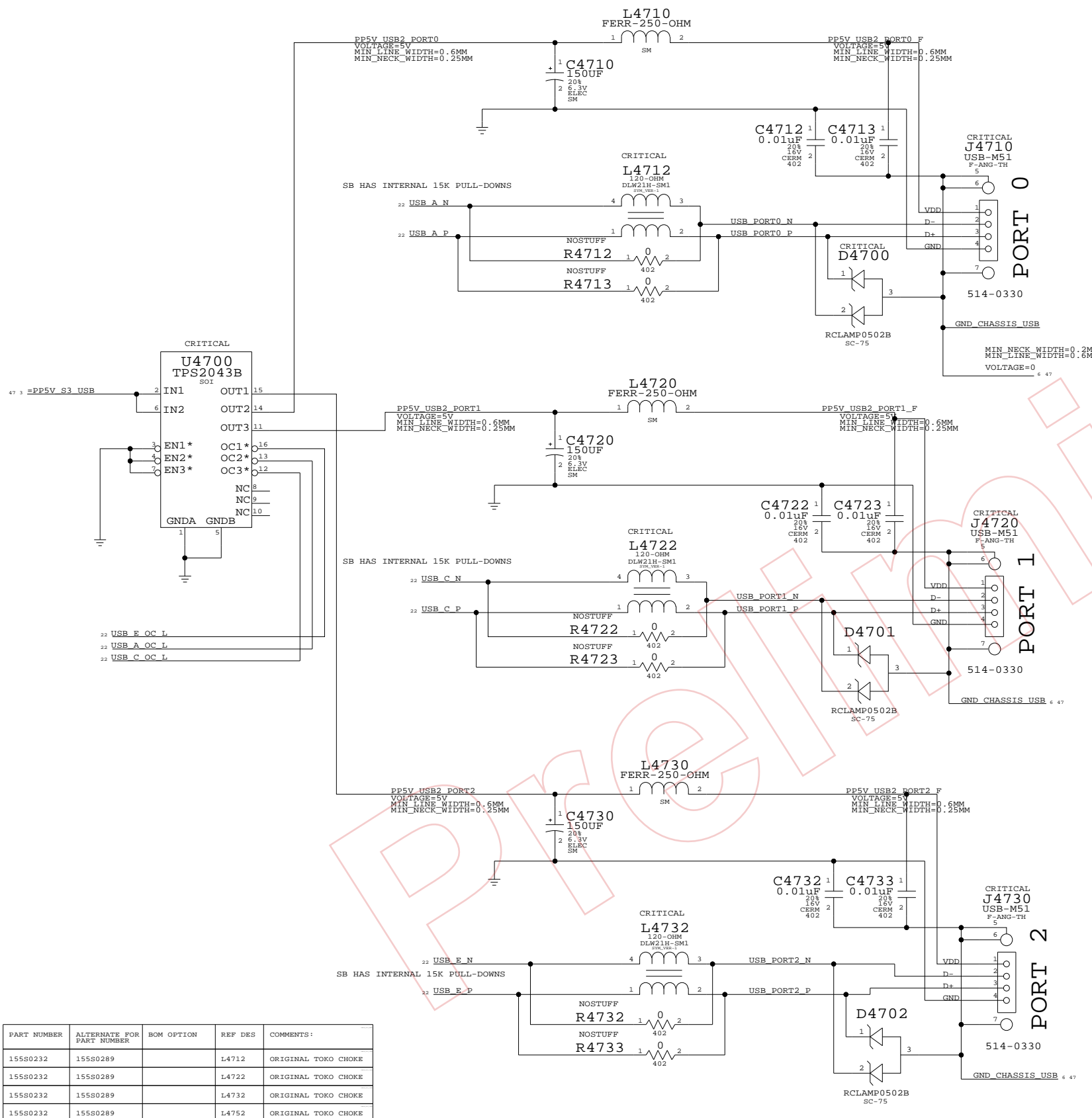
SCALE

NONE

SHT

46 OF 97

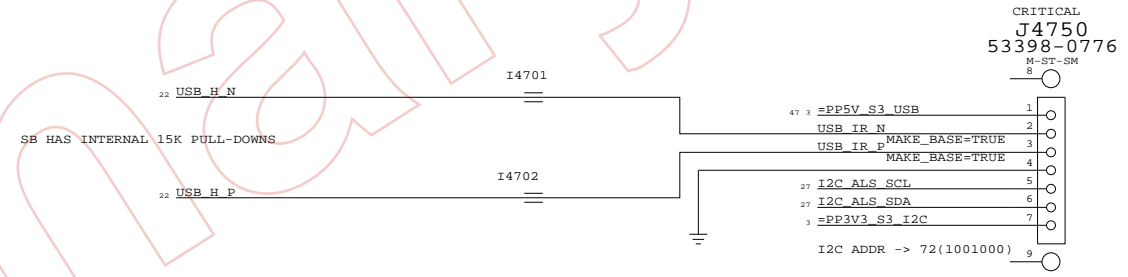
External USB Ports



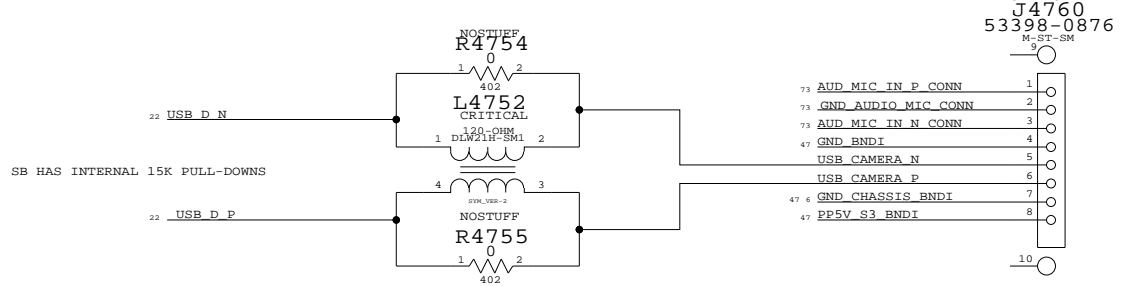
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		L4712	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4722	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4732	ORIGINAL TOKO CHOKE
155S0232	155S0289		L4752	ORIGINAL TOKO CHOKE

LAYOUT NOTE:
PLACE C4743, C4797 & L4740
NEAR J4760 PIN 8 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.
PLACE C4742 CLOSED TO J4760.

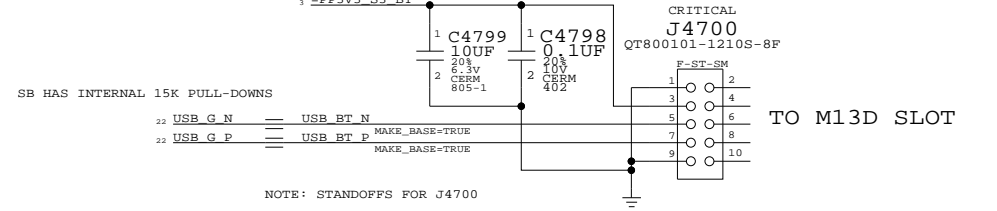
IR RECEIVER & ALS



CAMERA & MIC



BLUETOOTH



USB Device Interfaces

SYNC_MASTER=M51_D0UG SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

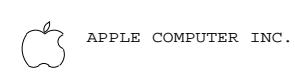
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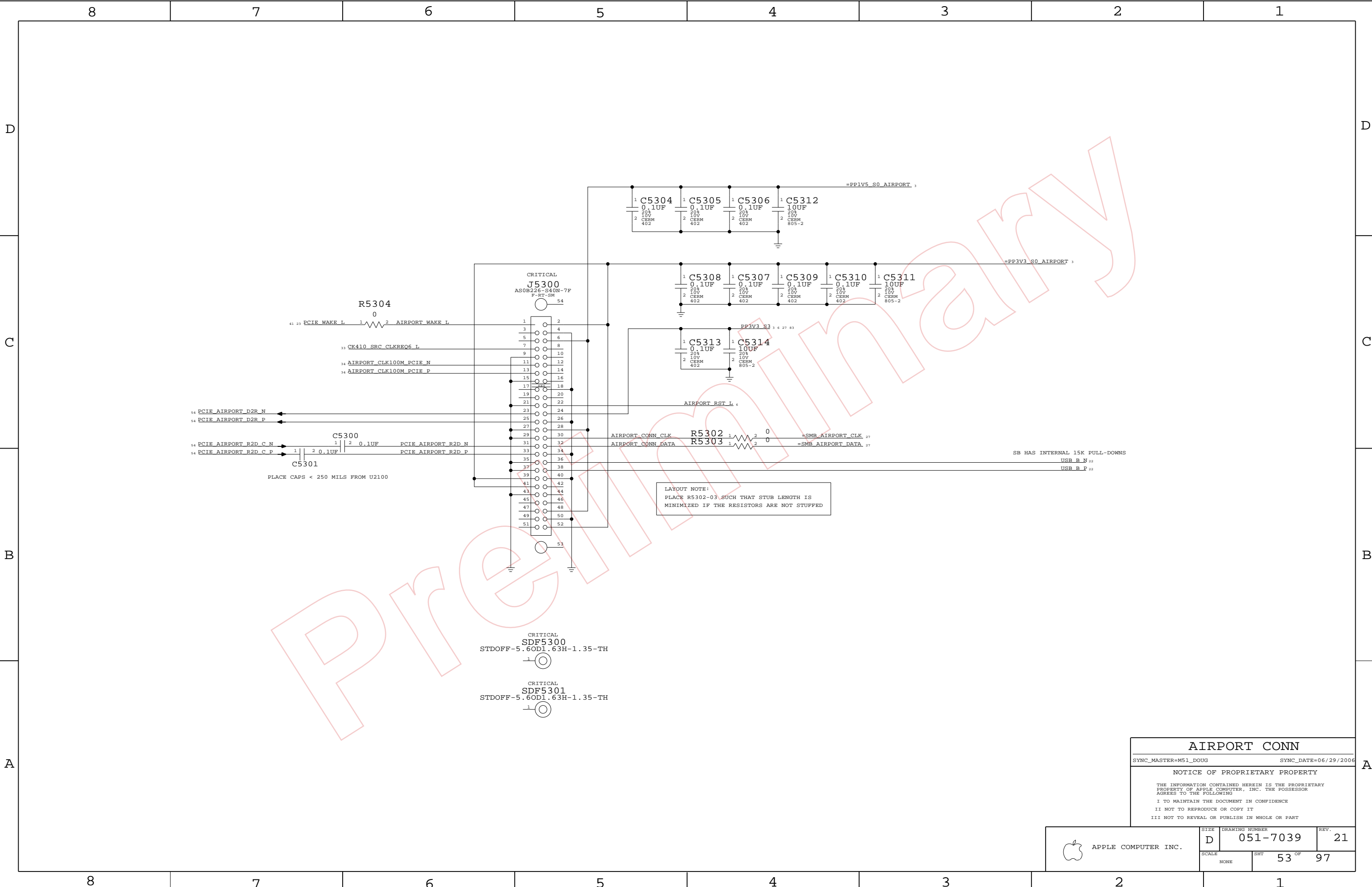
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SIZE	D	DRAWING NUMBER	051-7039	REV.	21
SCALE	NONE	SHT	47 OF 97		





AIRPORT CONN

SYNC_MASTER=M51_DOUG

SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

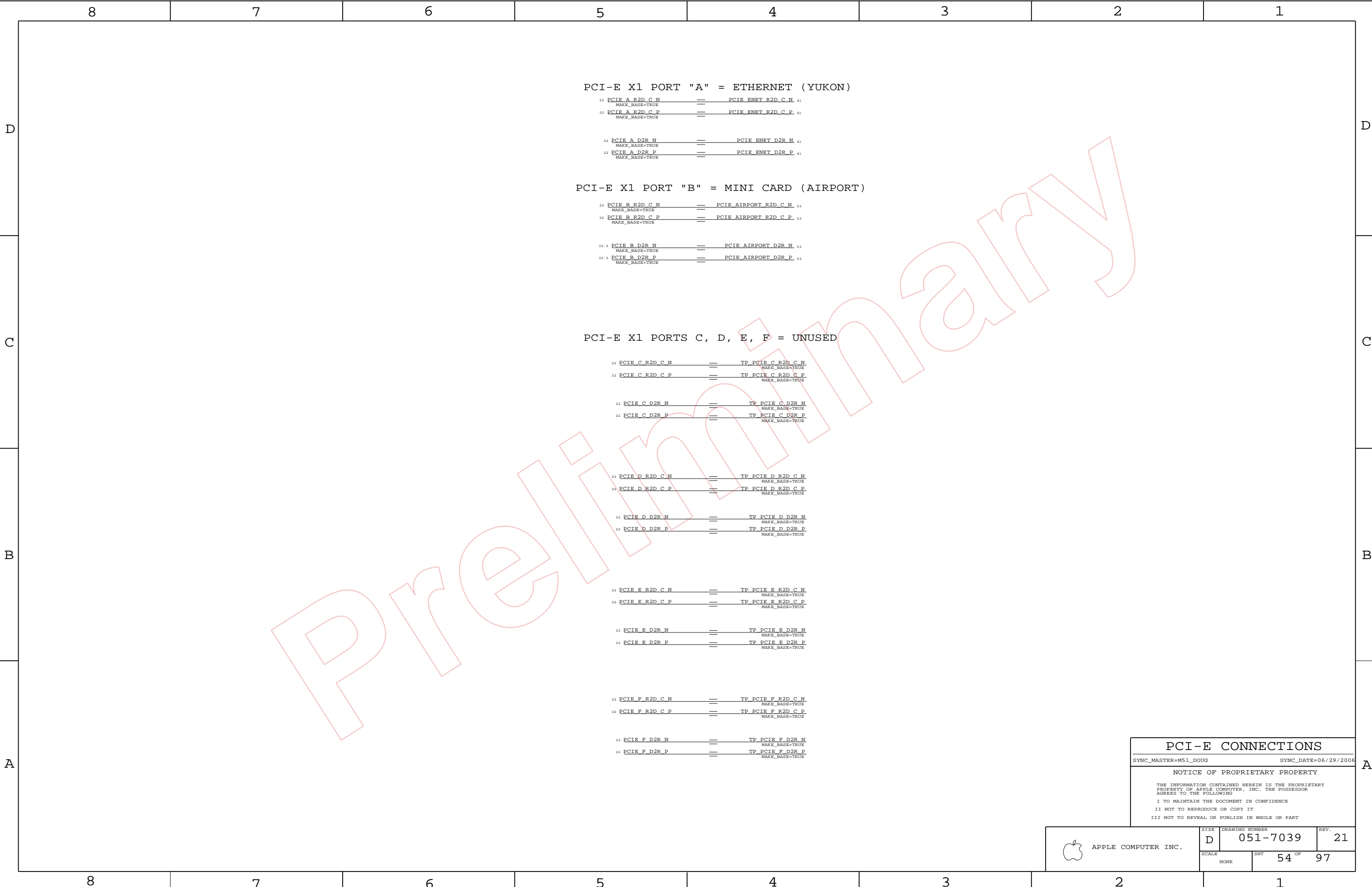
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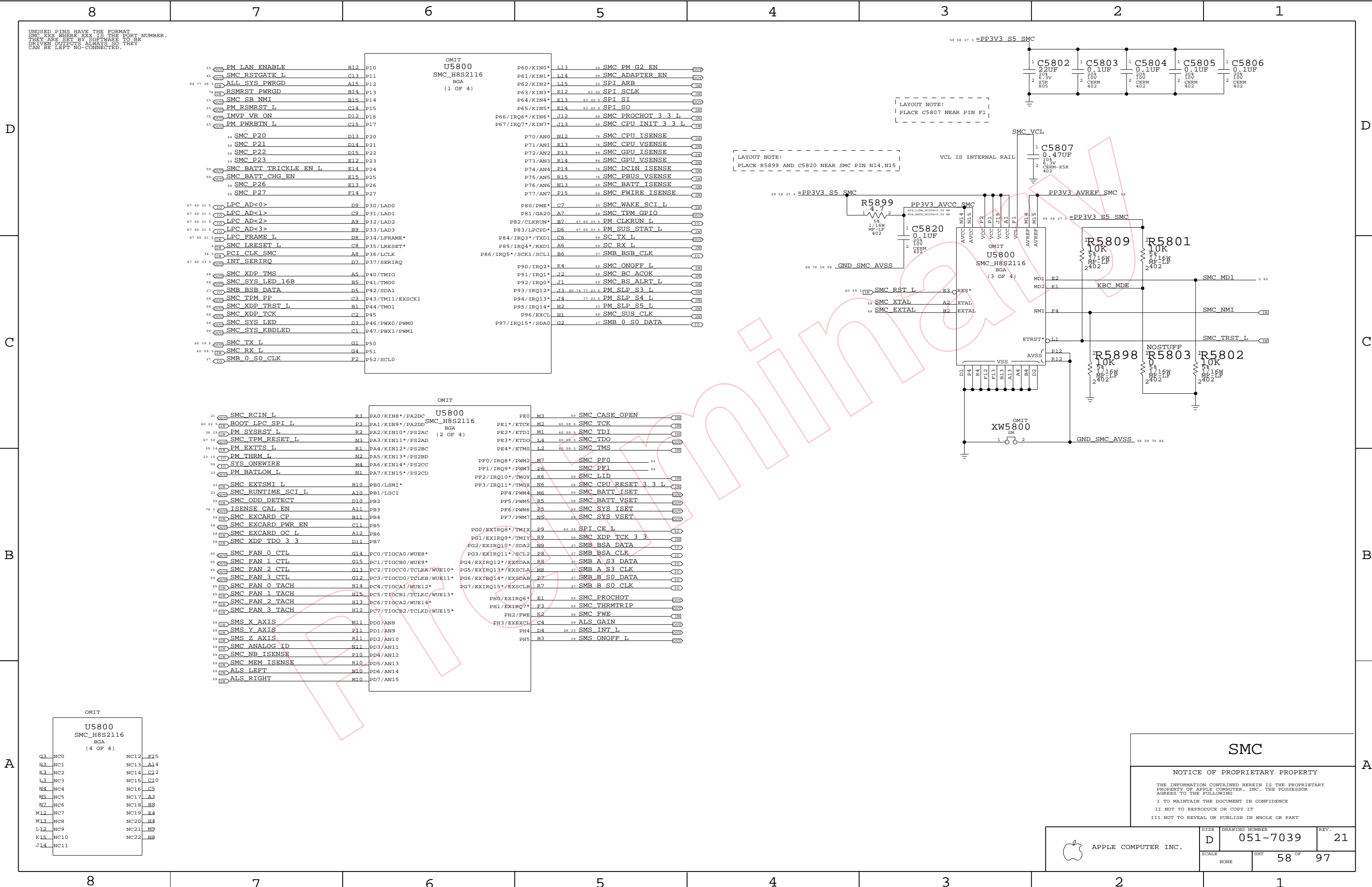
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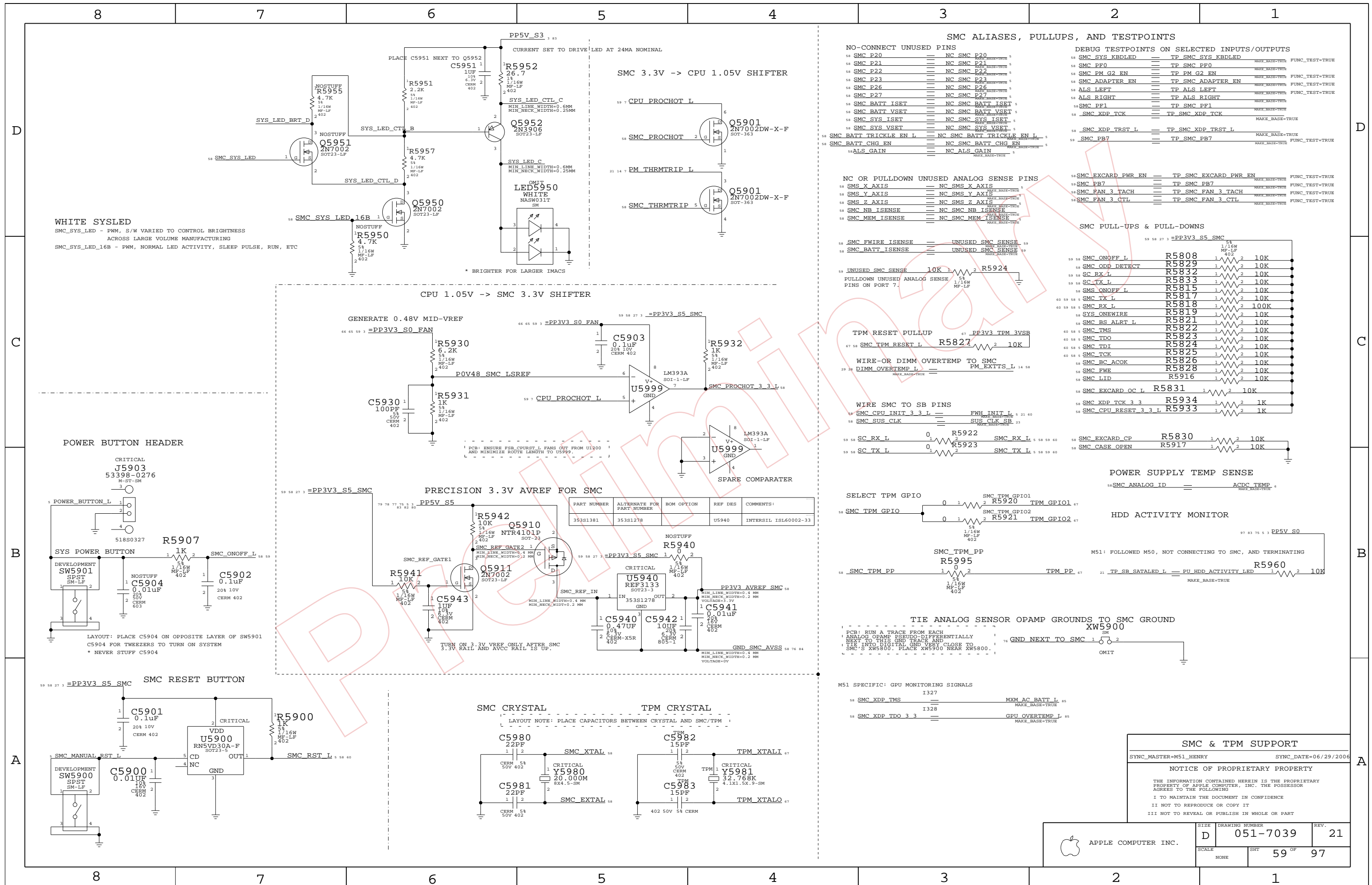
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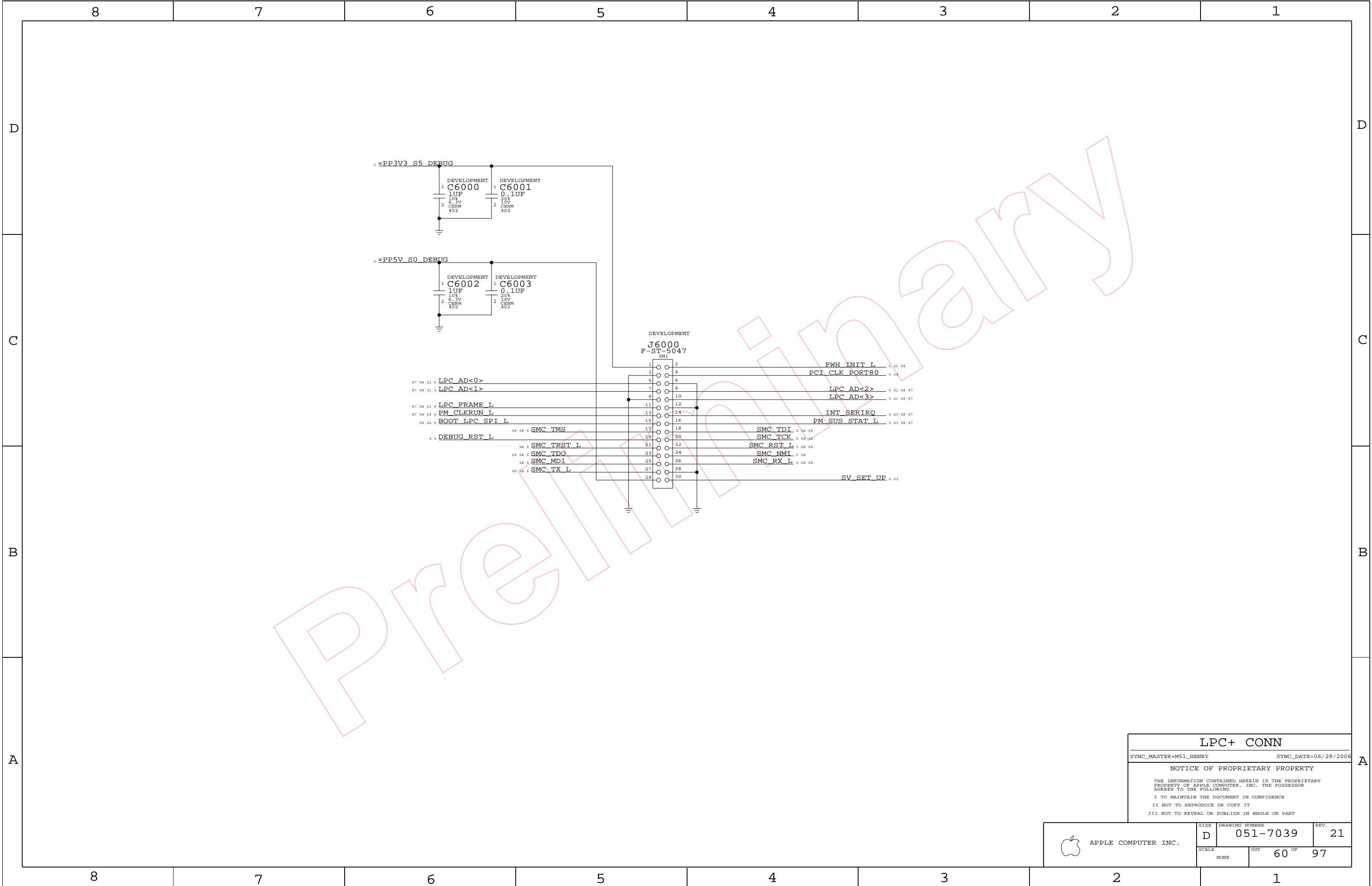
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

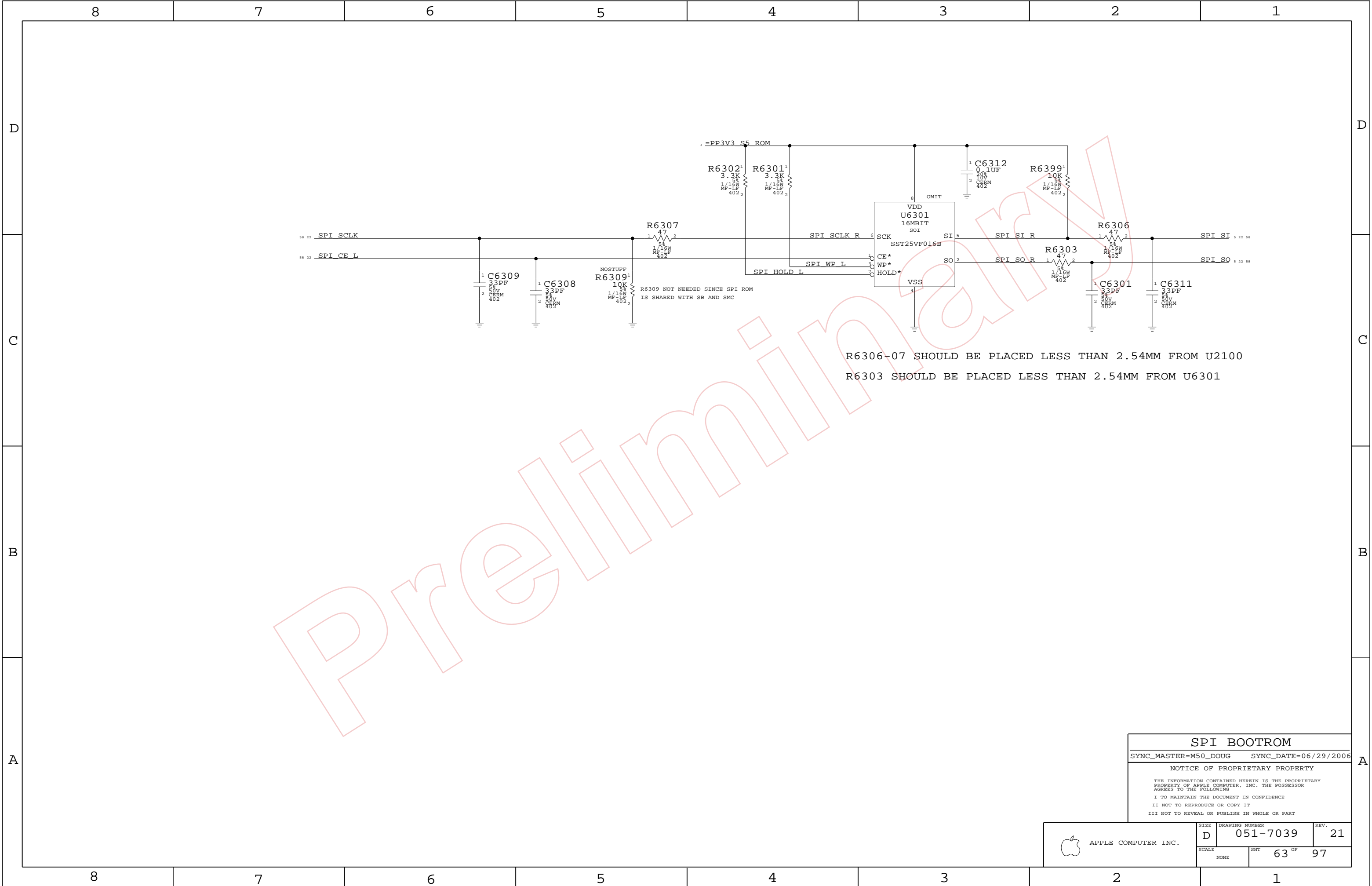
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	21
SCALE		SHT	53 OF 97
NONE			

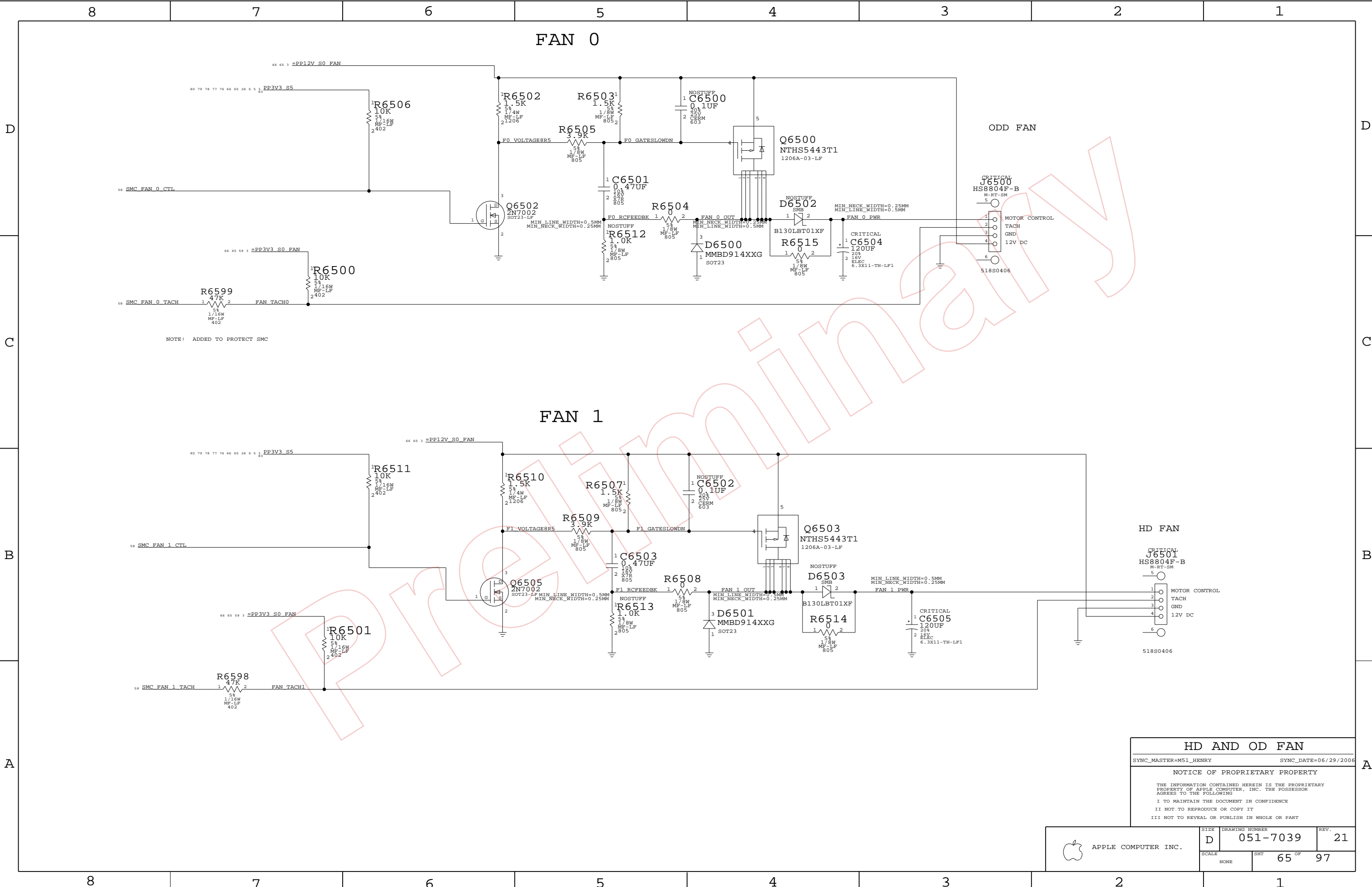












HD AND OD FAN

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

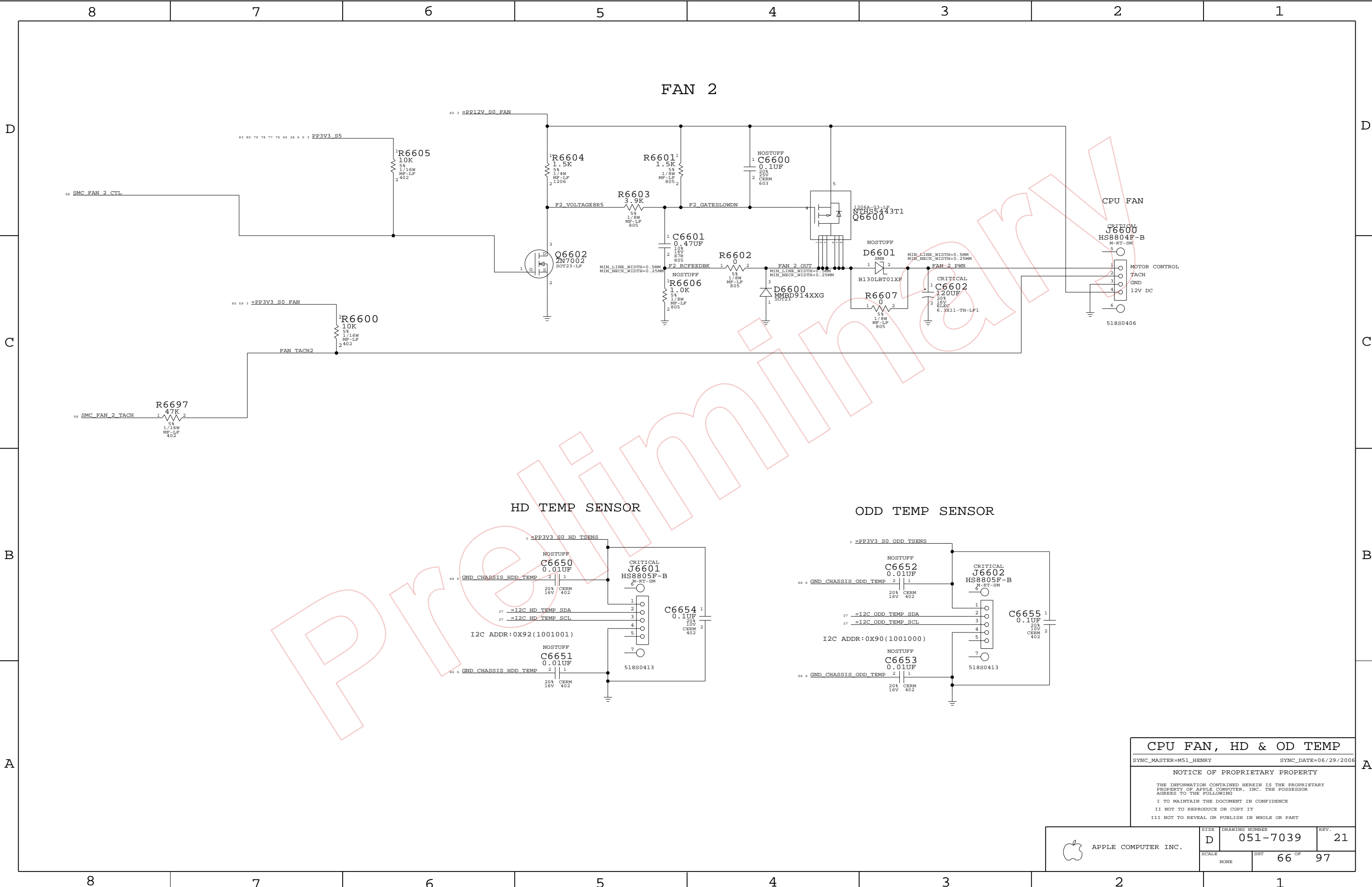
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	D	051-7039	21
SCALE		SHT	65 OF 97
NONE			



CPU FAN, HD & OD TEMP

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

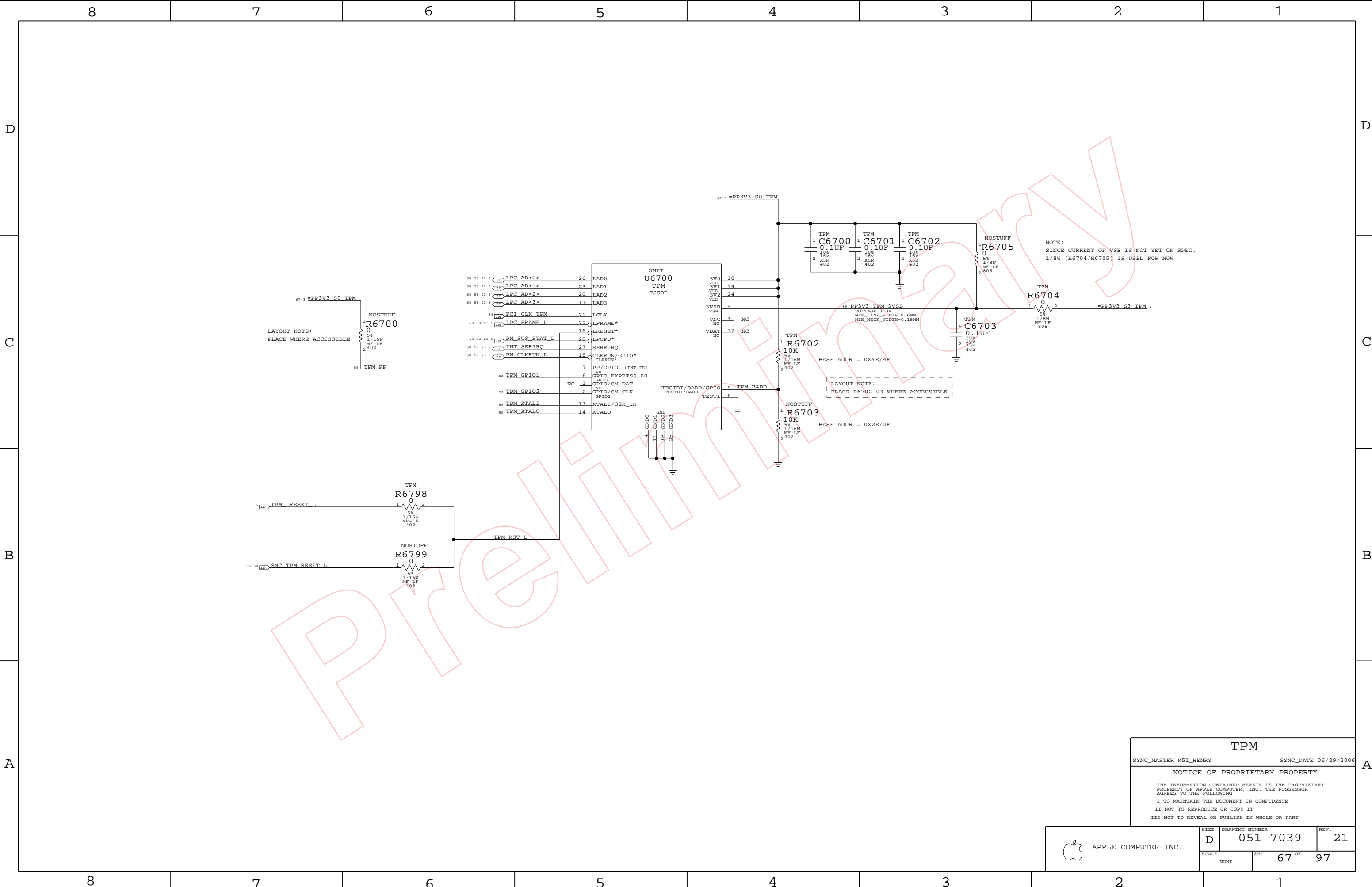
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	21
SCALE		SHT	66 OF 97
NONE			



TPM

SYNC_MASTER=M51_HENRY SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

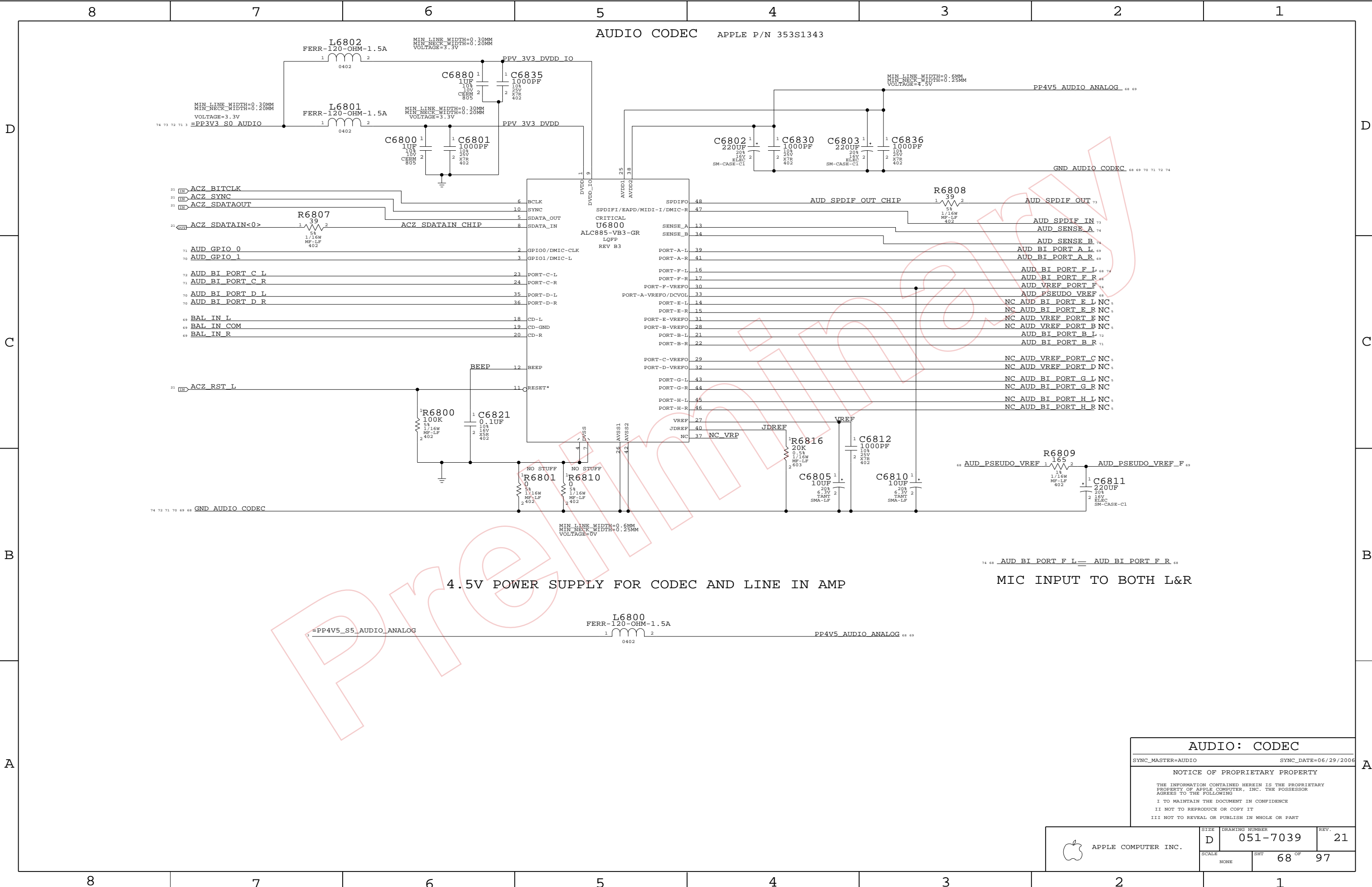
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	D	051-7039	21
SCALE		SHT	67 OF 97
NONE			



AUDIO: CODEC

SYNC_MASTER=AUDIO

SYNC_DATE=06/29/2006

NOTICE OF PROPRIETARY PROPERTY

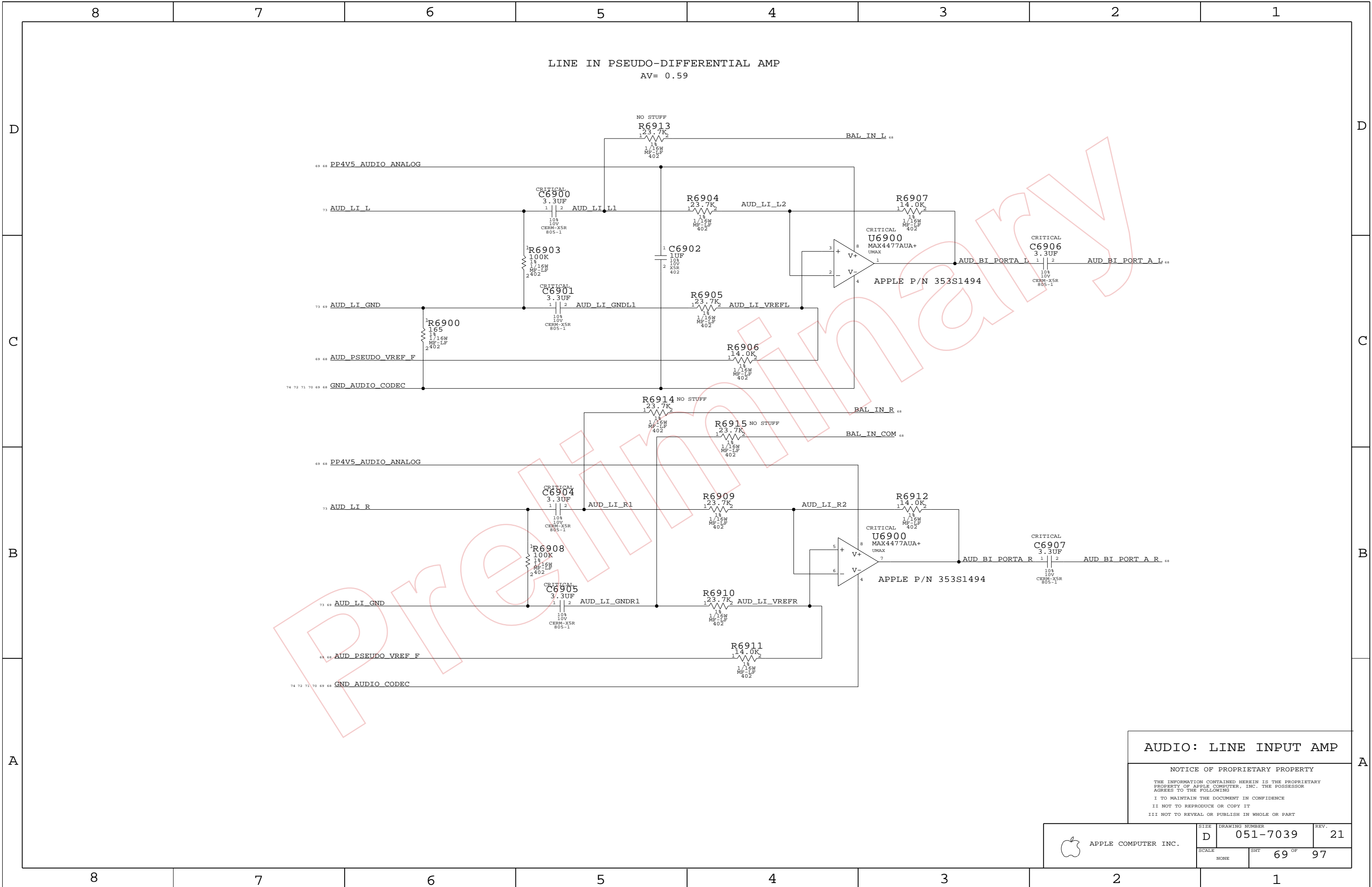
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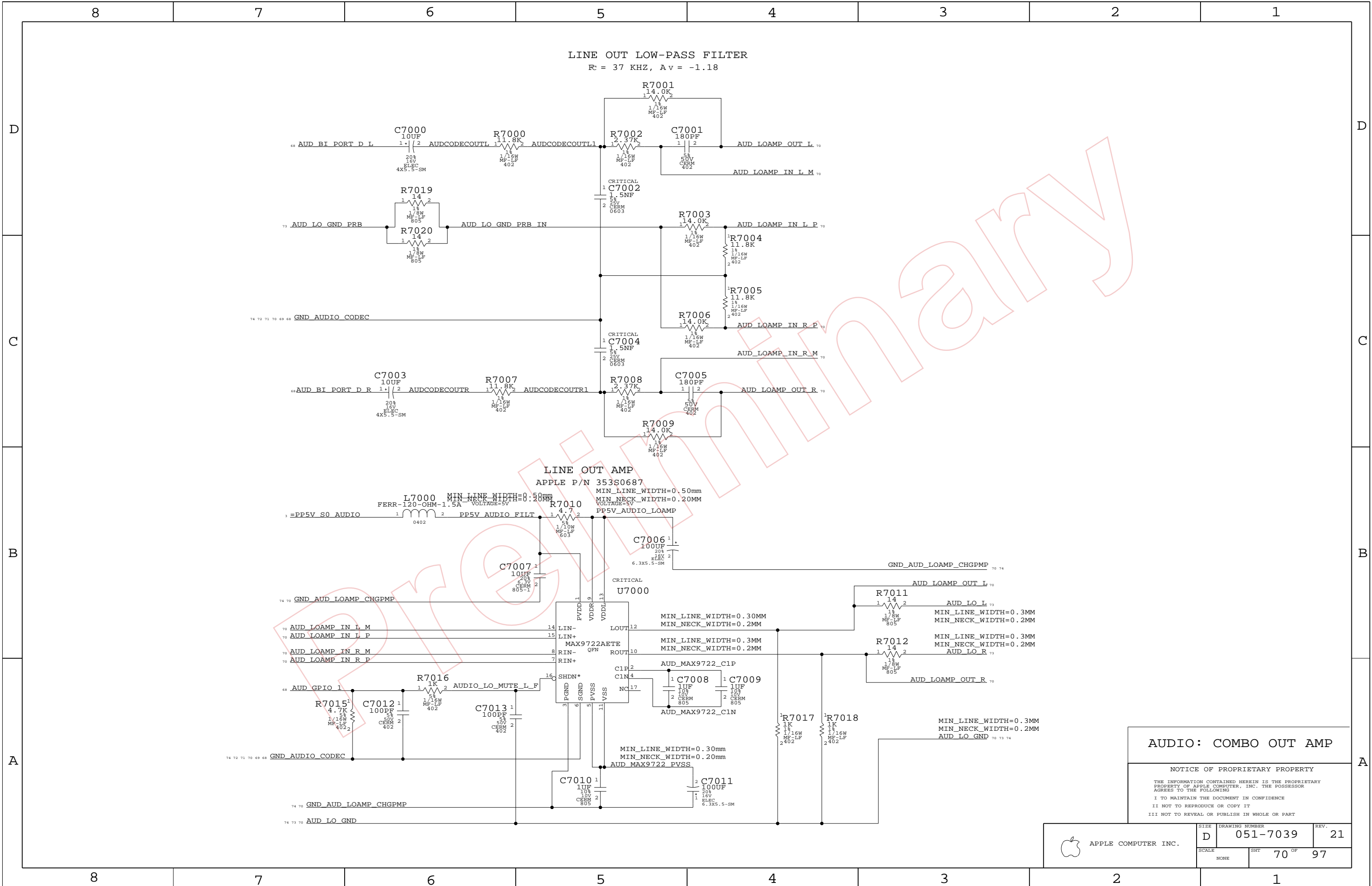
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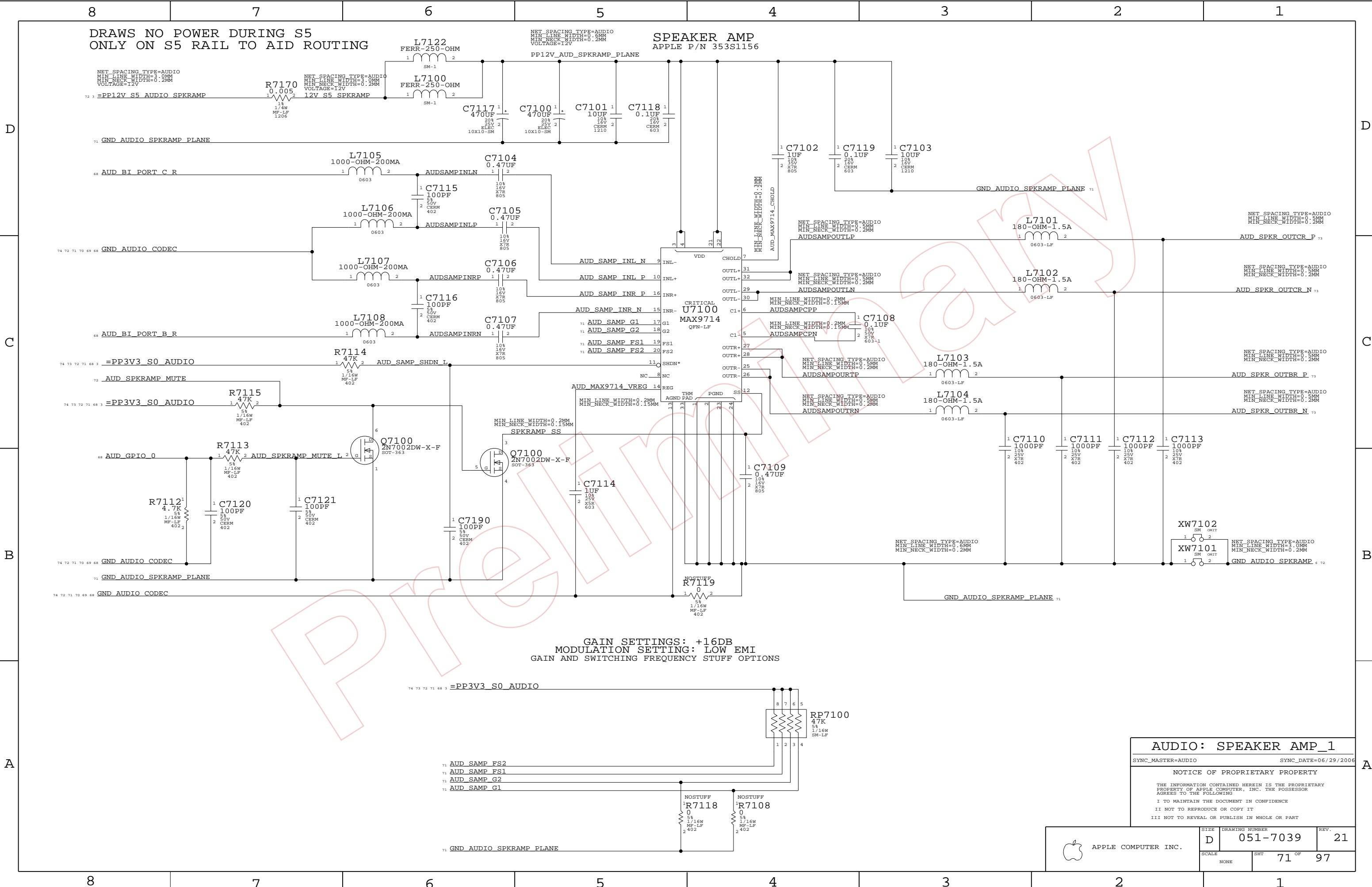
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	21
SCALE		SHT	68 OF 97
NONE			







AUDIO: SPEAKER AMP_1

SYNC_MASTER=AUDIO SYNC_DATE=06/29/2006

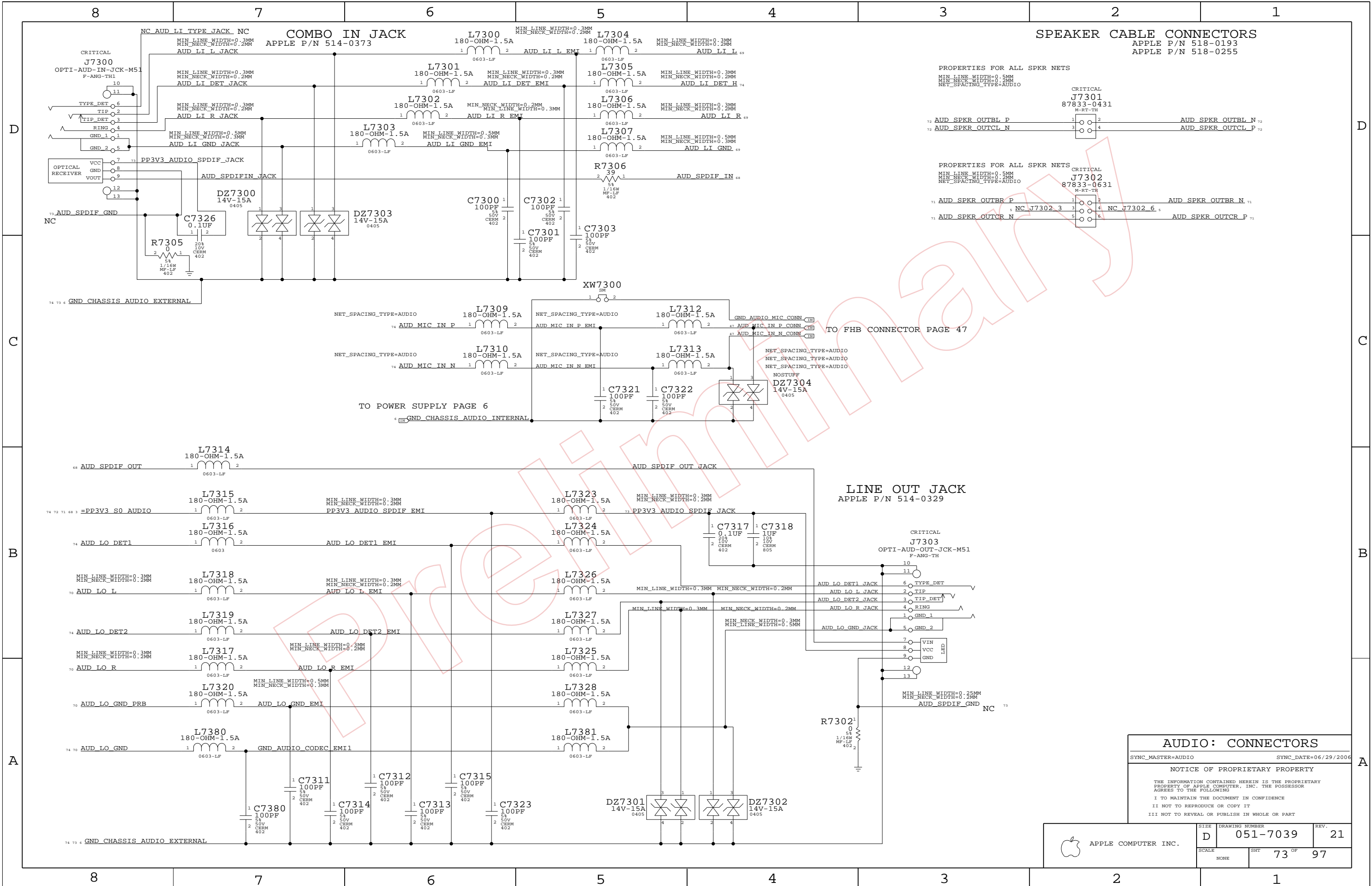
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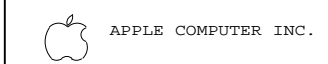
APPLE COMPUTER INC.

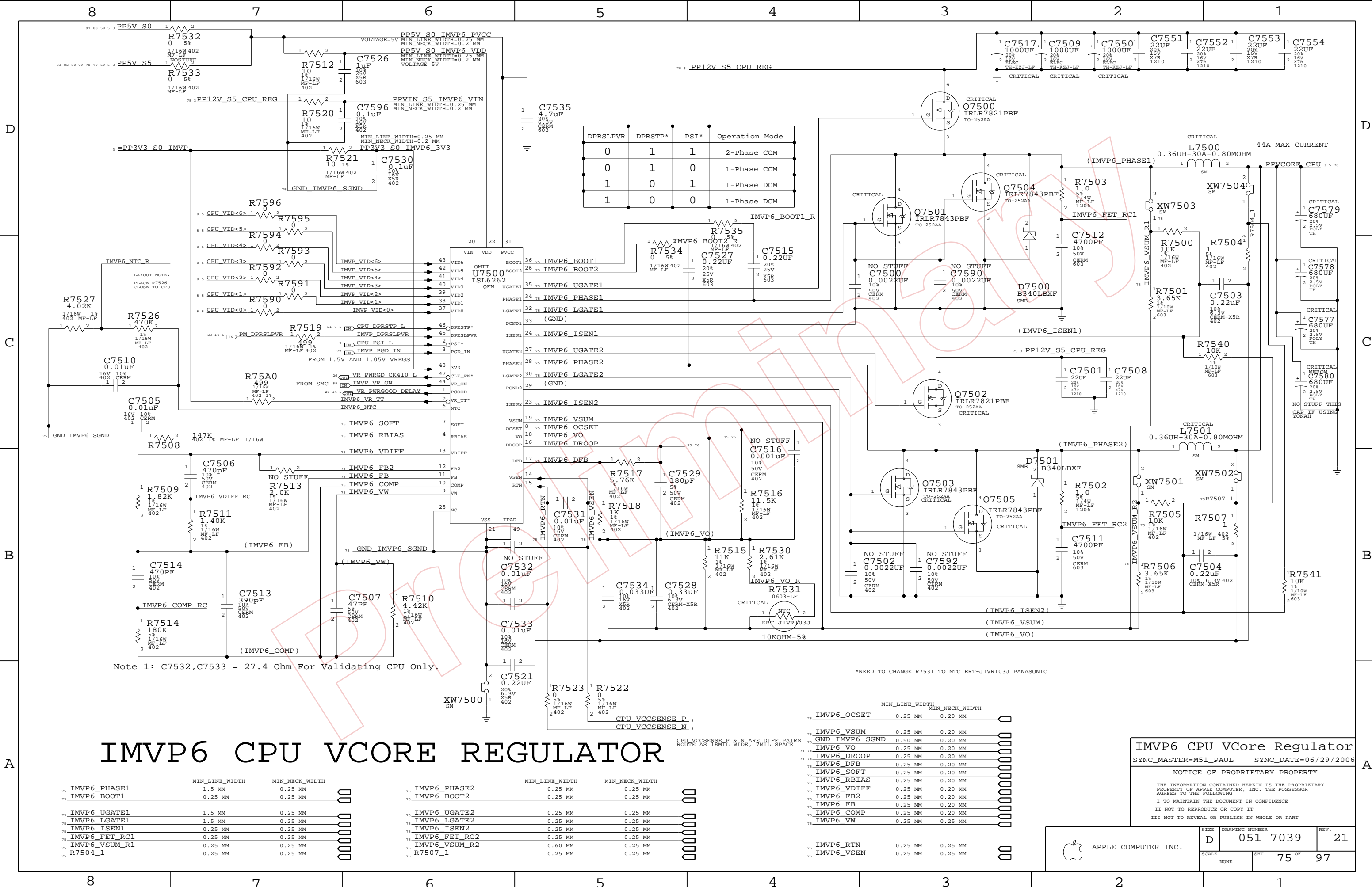
SIZE	DRAWING NUMBER	REV.
D	051-7039	21
SCALE	SHT	OF
NONE	71	97



AUDIO: CONNECTORS	
SYNC_MASTER=AUDIO	SYNC_DATE=06/29/2006
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DRAWING NUMBER	REV.	SCALE	
		SCALE	SHT
D 051-7039	21	NONE	73 OF 97





IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
R7504_1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.60 MM	0.25 MM
R7507_1	0.25 MM	0.25 MM

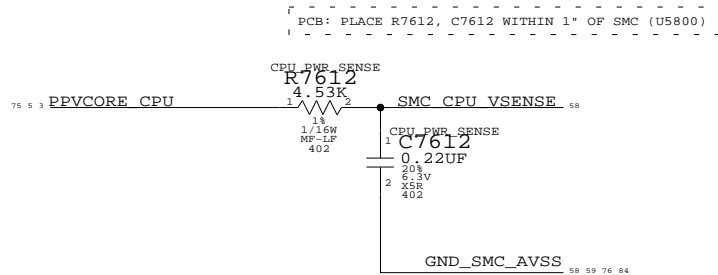
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

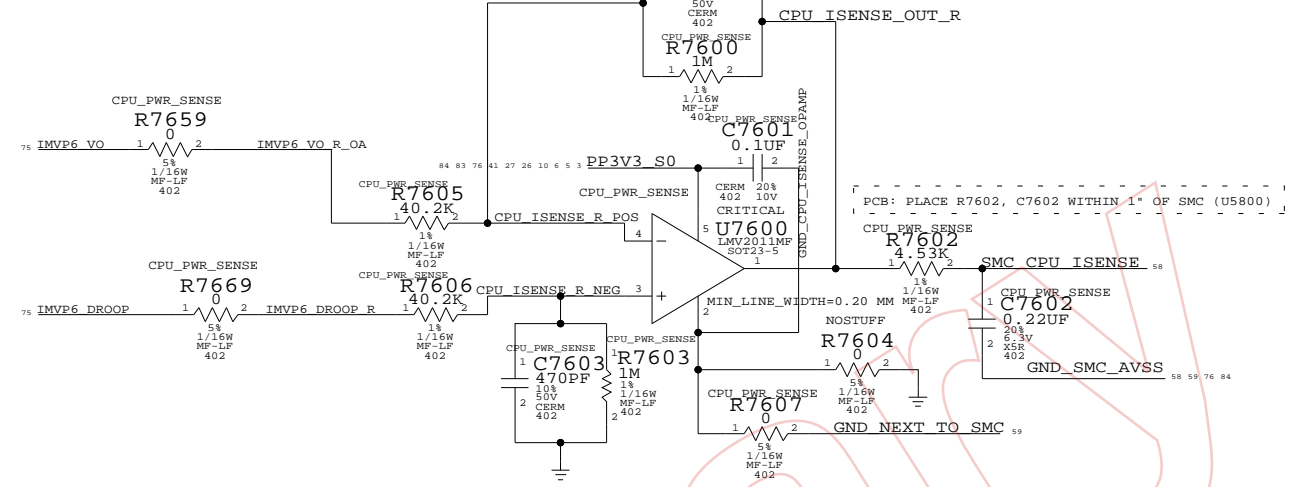
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7039	REV. 21
	SCALE NONE	SHT 75 OF 97	

PROCESSOR VCORE SENSE

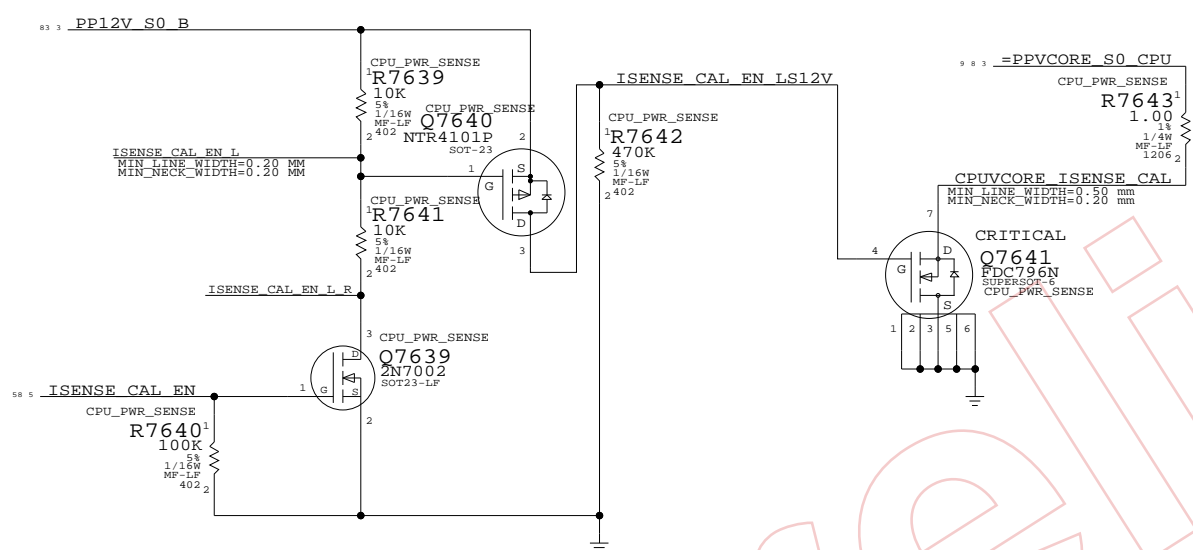


PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

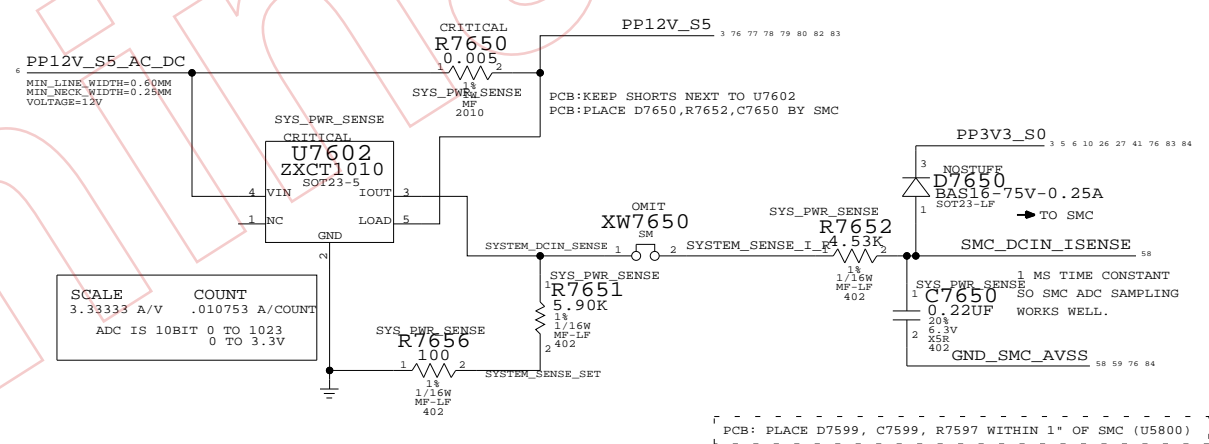


CPU CURRENT SENSE CALIBRATION CIRCUIT

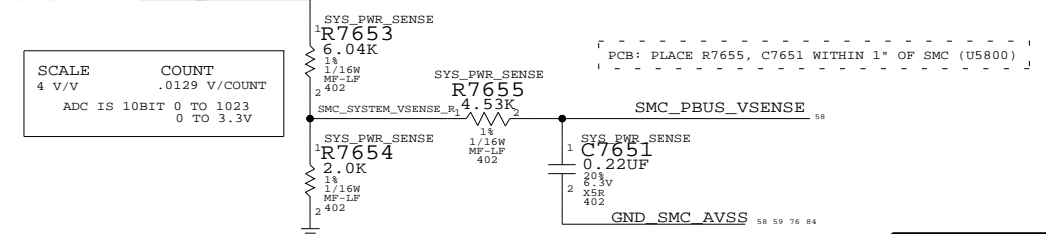
Switches in fixed load on power supplies to calibrate current sense circuits



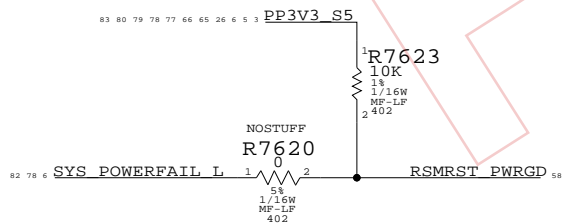
SYSTEM CURRENT SENSE



SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)



SMC PWRGD PULLUP

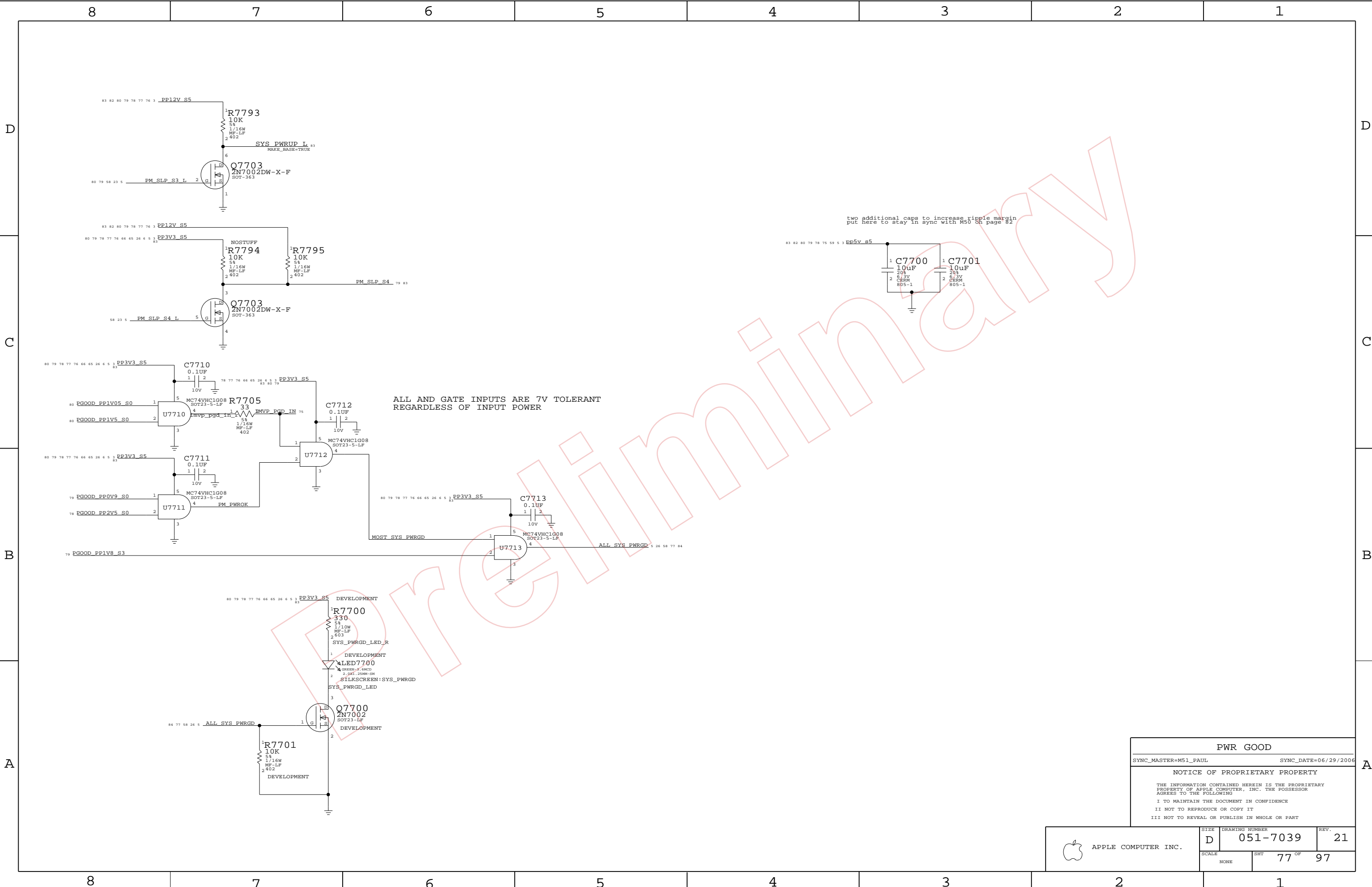


CPU & SYSTEM SENSE

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

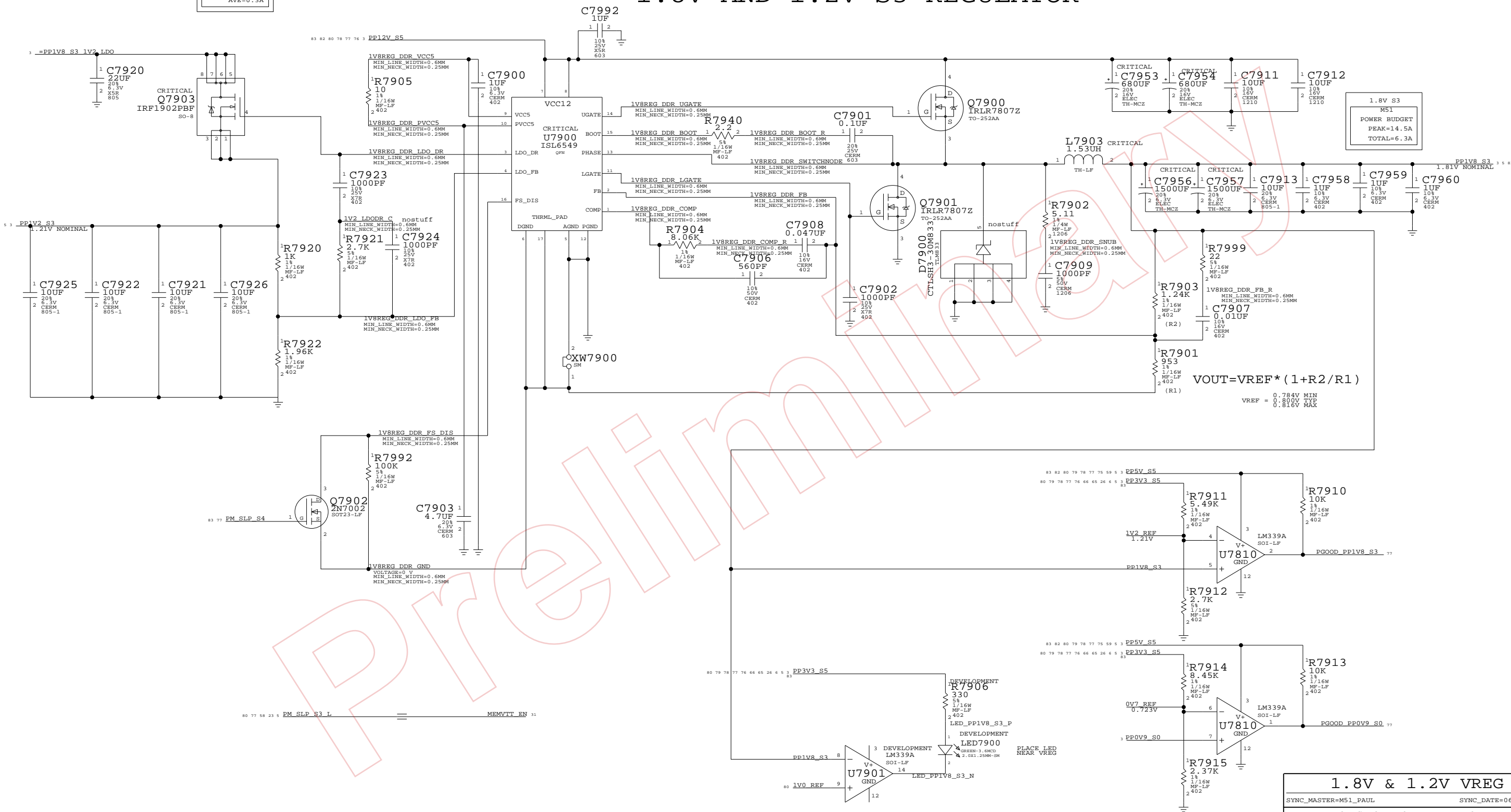
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PWR_GOOD		
SYNC_MASTER=M51_PAUL		SYNC_DATE=06/29/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7039	21
SCALE		SHT	77 OF 97
NONE			

1.8V AND 1.2V S3 REGULATOR



1.8V & 1.2V VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

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	D	051-7039	21
	SCALE	SHT	79 OF 97
	NONE		

1.5V S0 AND 1.05V S0 RAILS

D

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C

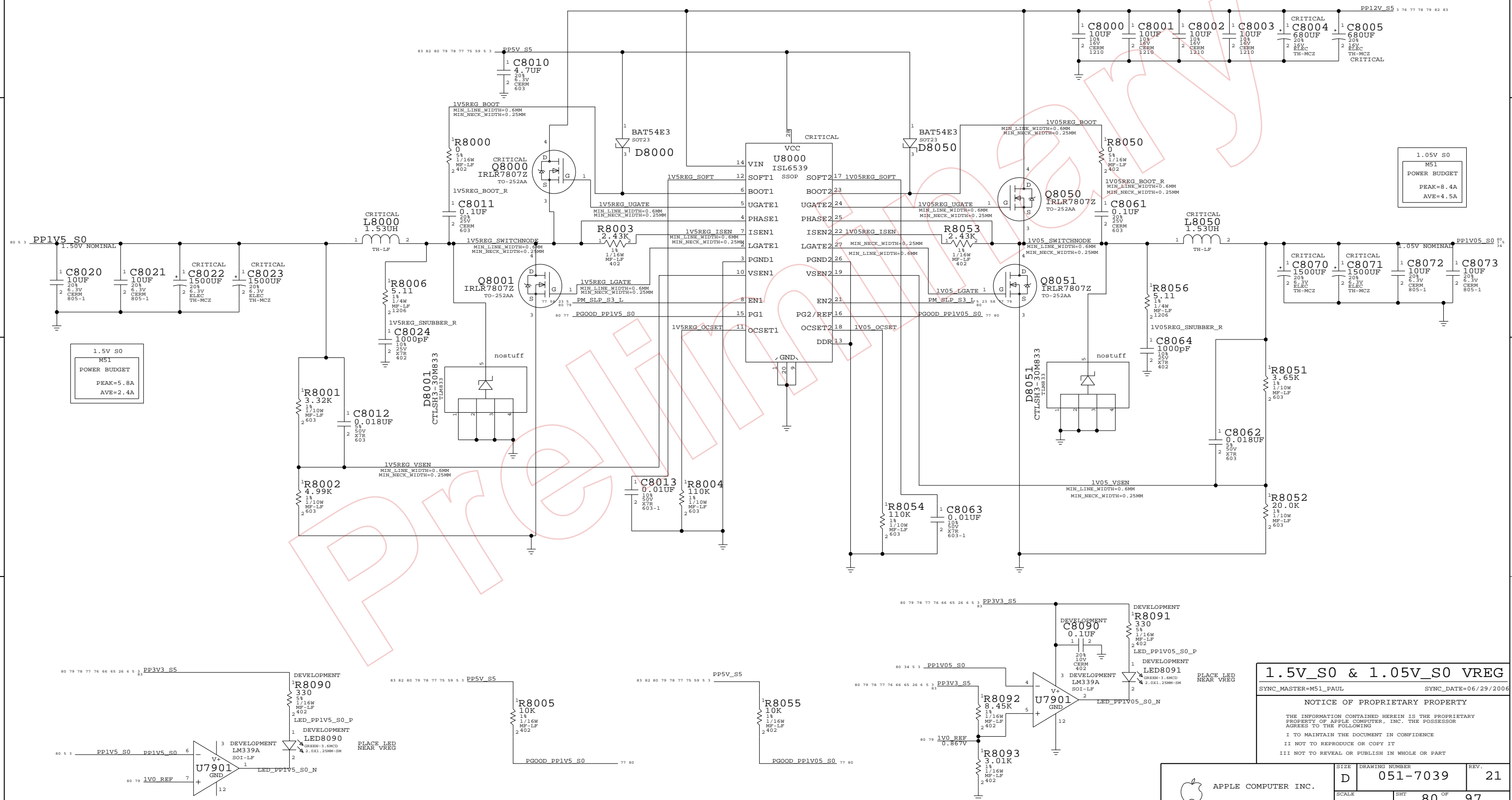
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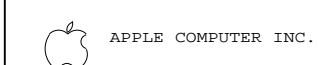


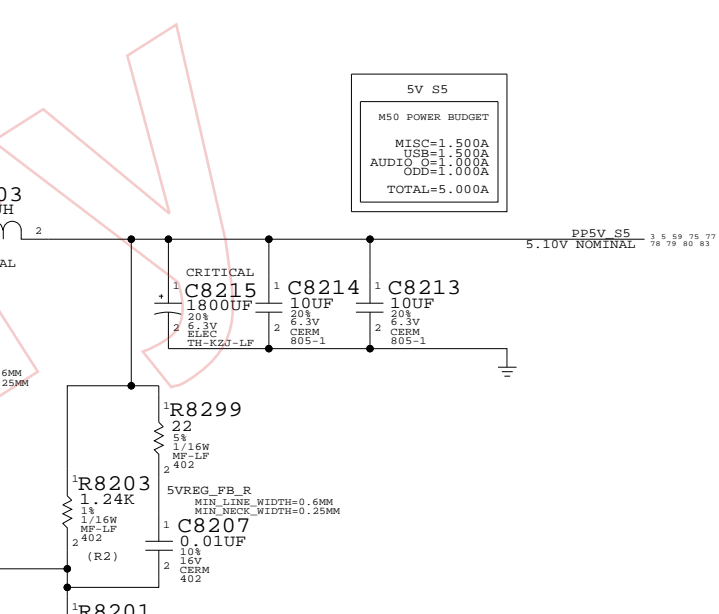
1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

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SIZE	D	DRAWING NUMBER	051-7039	REV.	21
SCALE	NONE	SHT	80 OF 97		



[illegible]

5V DC/DC

NOTICE OF PROPRIETARY PROPERTY

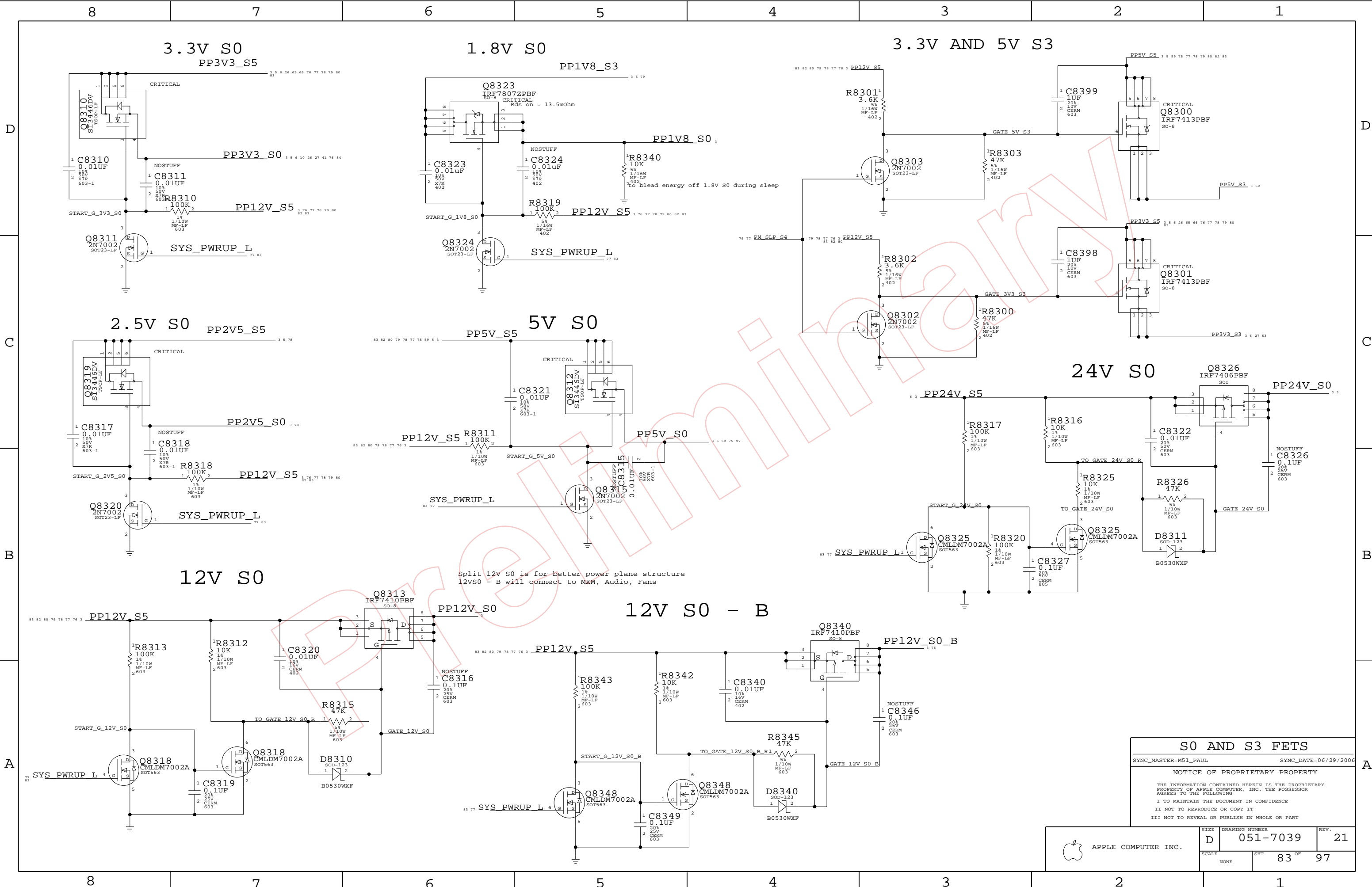
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
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SIZE	DRAWING NUMBER
D	051-7039

SIZE	DRAWING NUMBER	REV.
D	051-7039	21

SCALE	SHT	82	OF	95
NONE				



S0 AND S3 FETS

SYNC_MASTER=M51_PAUL SYNC_DATE=06/29/2006

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Page Notes

Power aliases required by this page:

- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

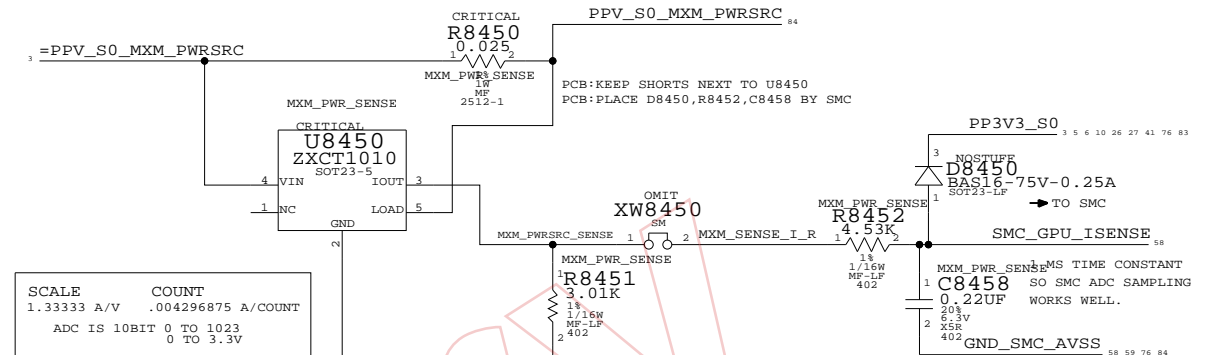
M51: FIX ON CARD ALLOWS US TO NOT STUFF MOST OF THE 1.8V DECOUPLING, WITH NO DROOP OR NOISE

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

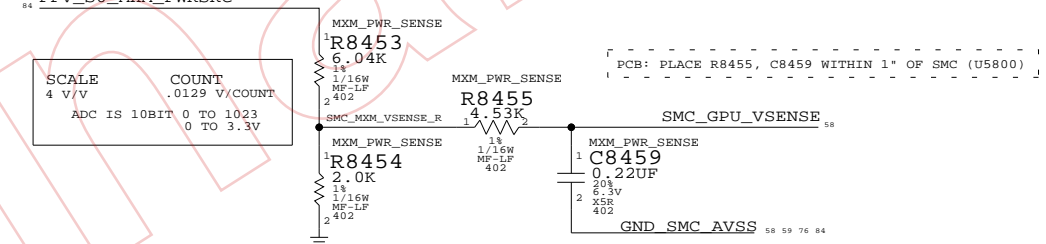
PLACE CAPS NEAR NB

REF	VALUE	UNIT	LOC	REF	VALUE	UNIT	LOC
133	PEG R2D C P<0>	C8420	0.1uF	109	PEG R2D P<15>		
133	PEG R2D C N<0>	C8421	0.1uF	1	PEG R2D N<15>		
133	PEG R2D C P<1>	C8422	0.1uF	1	PEG R2D P<14>		
133	PEG R2D C N<1>	C8423	0.1uF	1	PEG R2D N<14>		
133	PEG R2D C P<2>	C8424	0.1uF	1	PEG R2D P<13>		
133	PEG R2D C N<2>	C8425	0.1uF	1	PEG R2D N<13>		
133	PEG R2D C P<3>	C8426	0.1uF	1	PEG R2D P<12>		
133	PEG R2D C N<3>	C8427	0.1uF	1	PEG R2D N<12>		
133	PEG R2D C P<4>	C8428	0.1uF	1	PEG R2D P<11>		
133	PEG R2D C N<4>	C8429	0.1uF	1	PEG R2D N<11>		
133	PEG R2D C P<5>	C8430	0.1uF	1	PEG R2D P<10>		
133	PEG R2D C N<5>	C8431	0.1uF	1	PEG R2D N<10>		
133	PEG R2D C P<6>	C8432	0.1uF	1	PEG R2D P<9>		
133	PEG R2D C N<6>	C8433	0.1uF	1	PEG R2D N<9>		
133	PEG R2D C P<7>	C8434	0.1uF	1	PEG R2D P<8>		
133	PEG R2D C N<7>	C8435	0.1uF	1	PEG R2D N<8>		
133	PEG R2D C P<8>	C8436	0.1uF	1	PEG R2D P<7>		
133	PEG R2D C N<8>	C8437	0.1uF	1	PEG R2D N<7>		
133	PEG R2D C P<9>	C8438	0.1uF	1	PEG R2D P<6>		
133	PEG R2D C N<9>	C8439	0.1uF	1	PEG R2D N<6>		
133	PEG R2D C P<10>	C8440	0.1uF	1	PEG R2D P<5>		
133	PEG R2D C N<10>	C8441	0.1uF	1	PEG R2D N<5>		
133	PEG R2D C P<11>	C8442	0.1uF	1	PEG R2D P<4>		
133	PEG R2D C N<11>	C8443	0.1uF	1	PEG R2D N<4>		
133	PEG R2D C P<12>	C8444	0.1uF	1	PEG R2D P<3>		
133	PEG R2D C N<12>	C8445	0.1uF	1	PEG R2D N<3>		
133	PEG R2D C P<13>	C8446	0.1uF	1	PEG R2D P<2>		
133	PEG R2D C N<13>	C8447	0.1uF	1	PEG R2D N<2>		
133	PEG R2D C P<14>	C8448	0.1uF	1	PEG R2D P<1>		
133	PEG R2D C N<14>	C8449	0.1uF	1	PEG R2D N<1>		
133	PEG R2D C P<15>	C8450	0.1uF	1	PEG R2D P<0>		
133	PEG R2D C N<15>	C8451	0.1uF	1	PEG R2D N<0>		

MXM PWRSRC (GPU CORE) CURRENT SENSE



MXM PWRSRC VOLTAGE SENSE (SCALING 12V INPUT VOLTAGE TO SMC)



MXM PCI-E & PWR

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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D	051-7039	21
SCALE	SHT	84 OF 97
NONE		

Page Notes

Power aliases required by this page:

- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:

- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

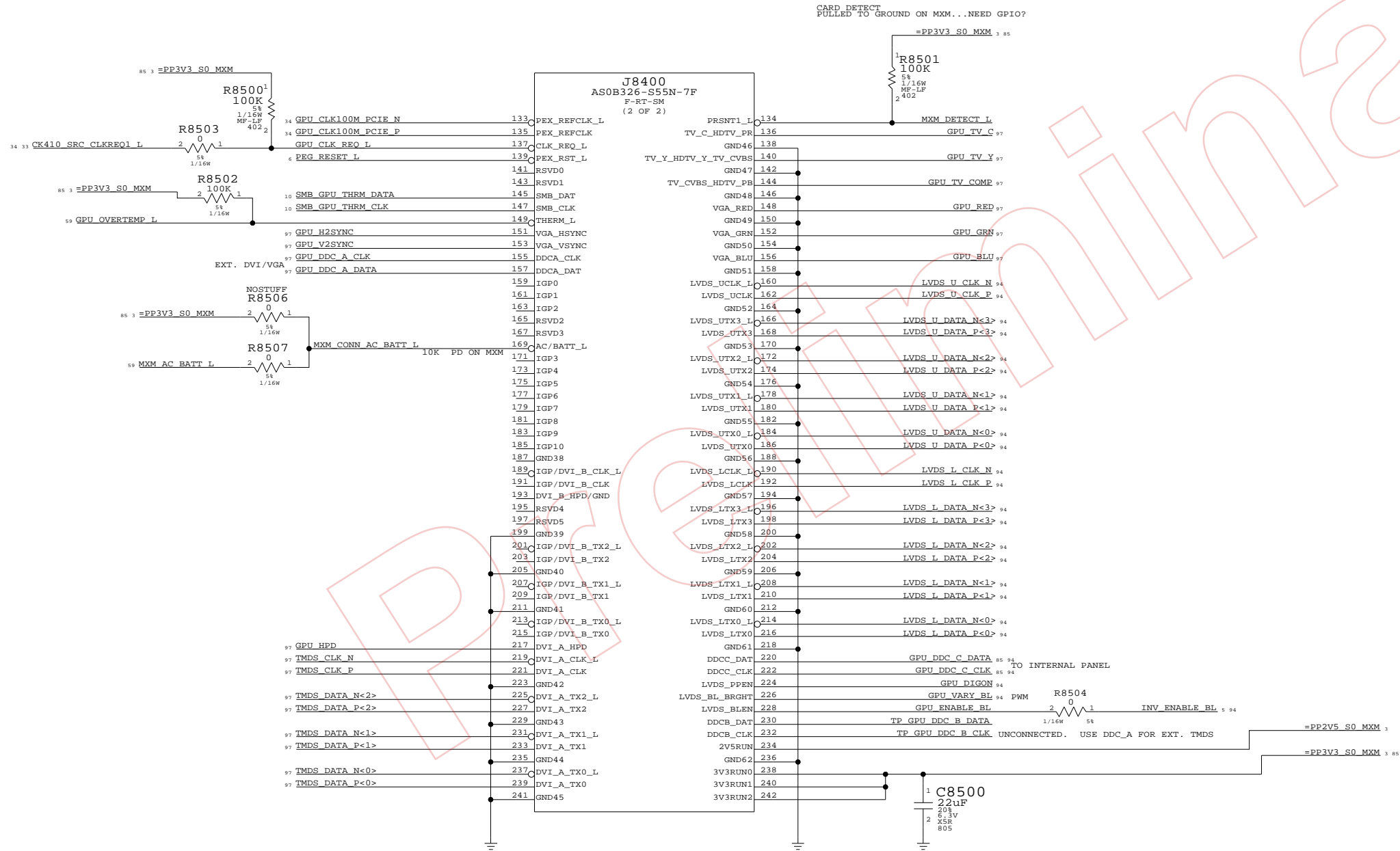
BOM options provided by this page:

(NONE)

MXM SPEC POWER REQUIREMENTS

(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT



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051-7039

REV.

21

SCALE

NONE

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85 OF 97

MXM I/O

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

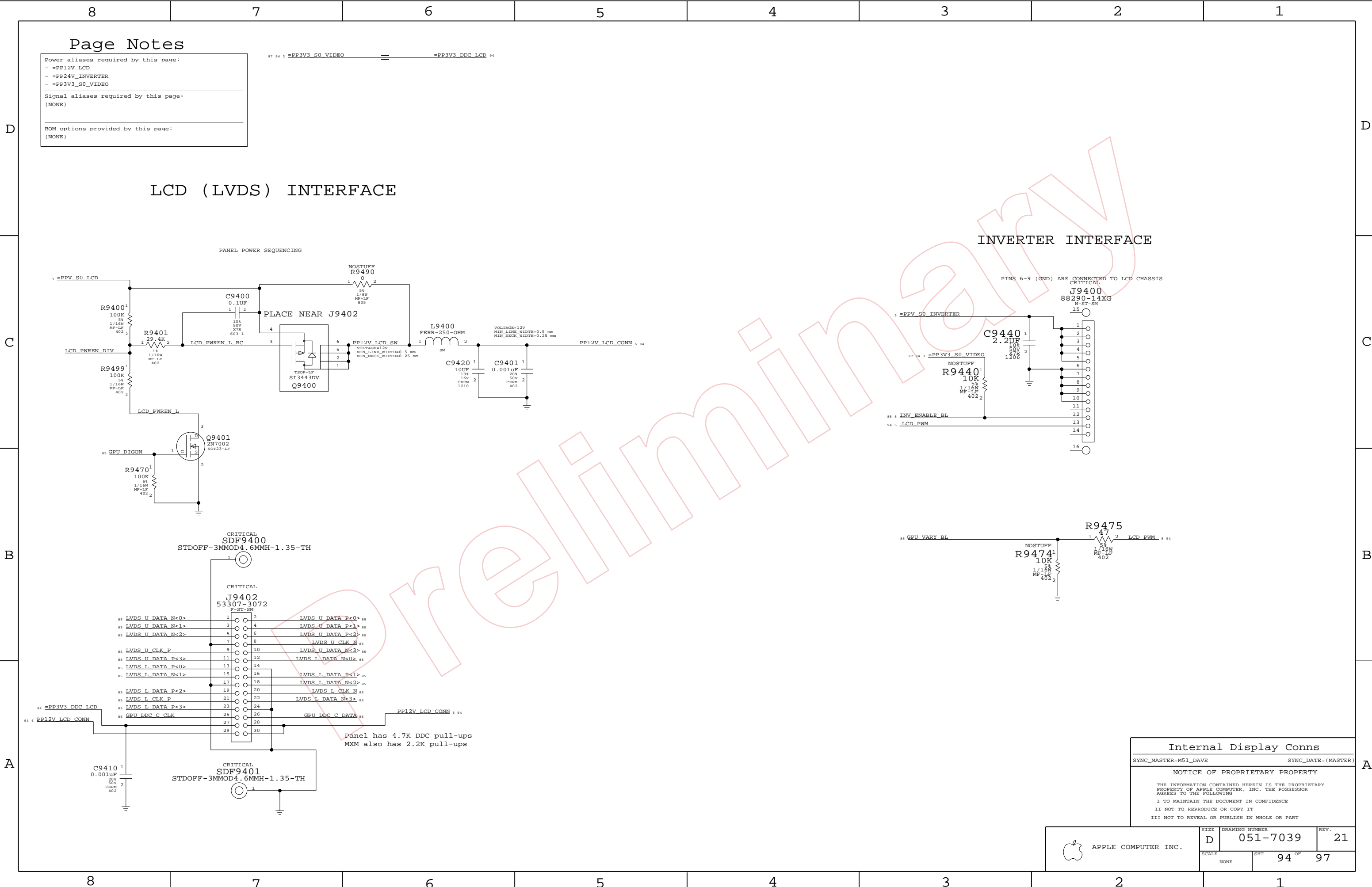
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Page Notes

Power aliases required by this page:

- =PP12V_LCD
- =PP24V_INVERTER
- =PP3V3_S0_VIDEO

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

LCD (LVDS) INTERFACE

INVERTER INTERFACE

Internal Display Conns

SYNC_MASTER=M51_DAVE SYNC_DATE=(MASTER)

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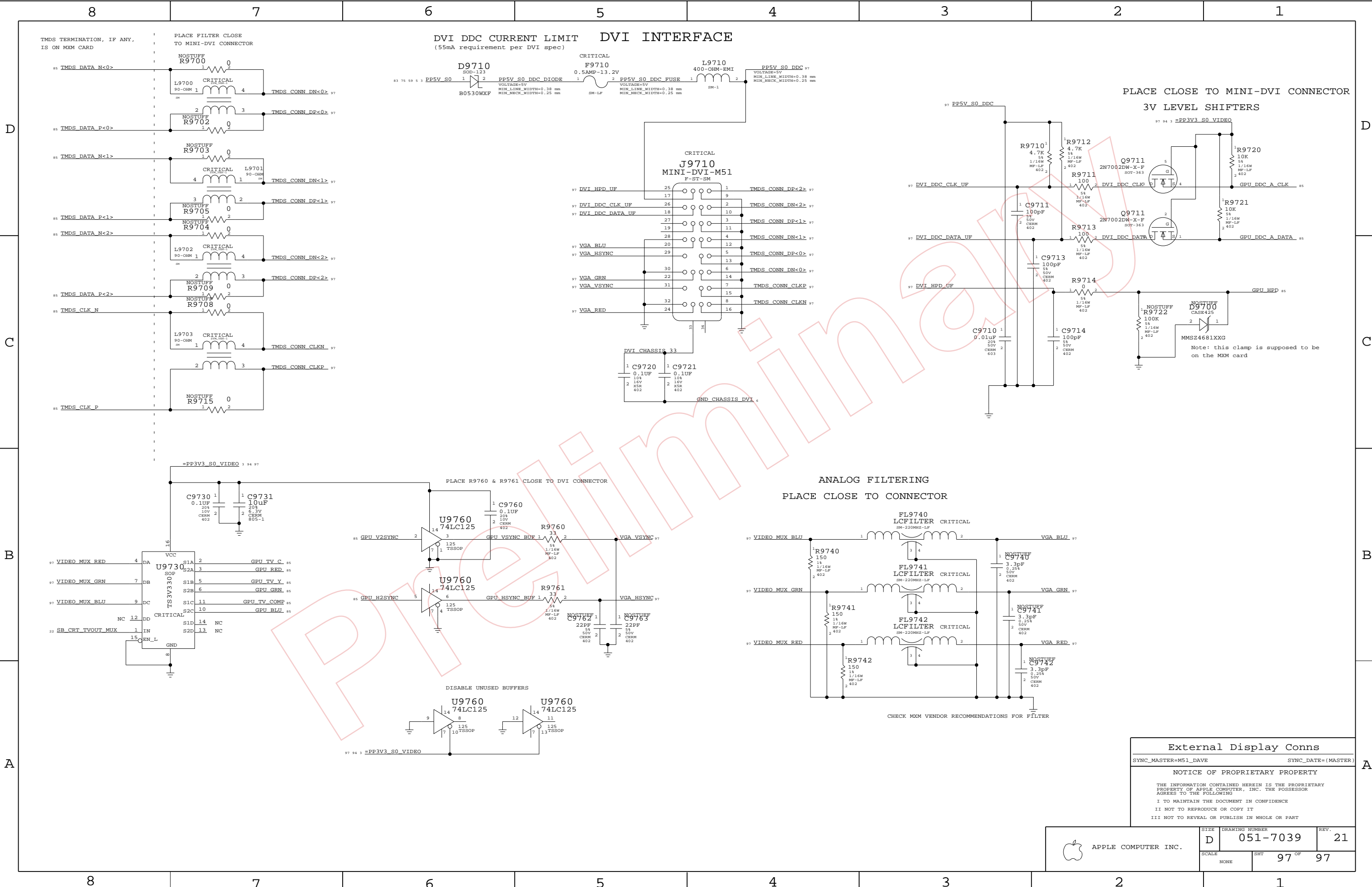
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NONE		



External Display Conns		
SYNC_MASTER=M51_DAVE		SYNC_DATE=(MASTER)
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SCALE		SHT	97 OF 97
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